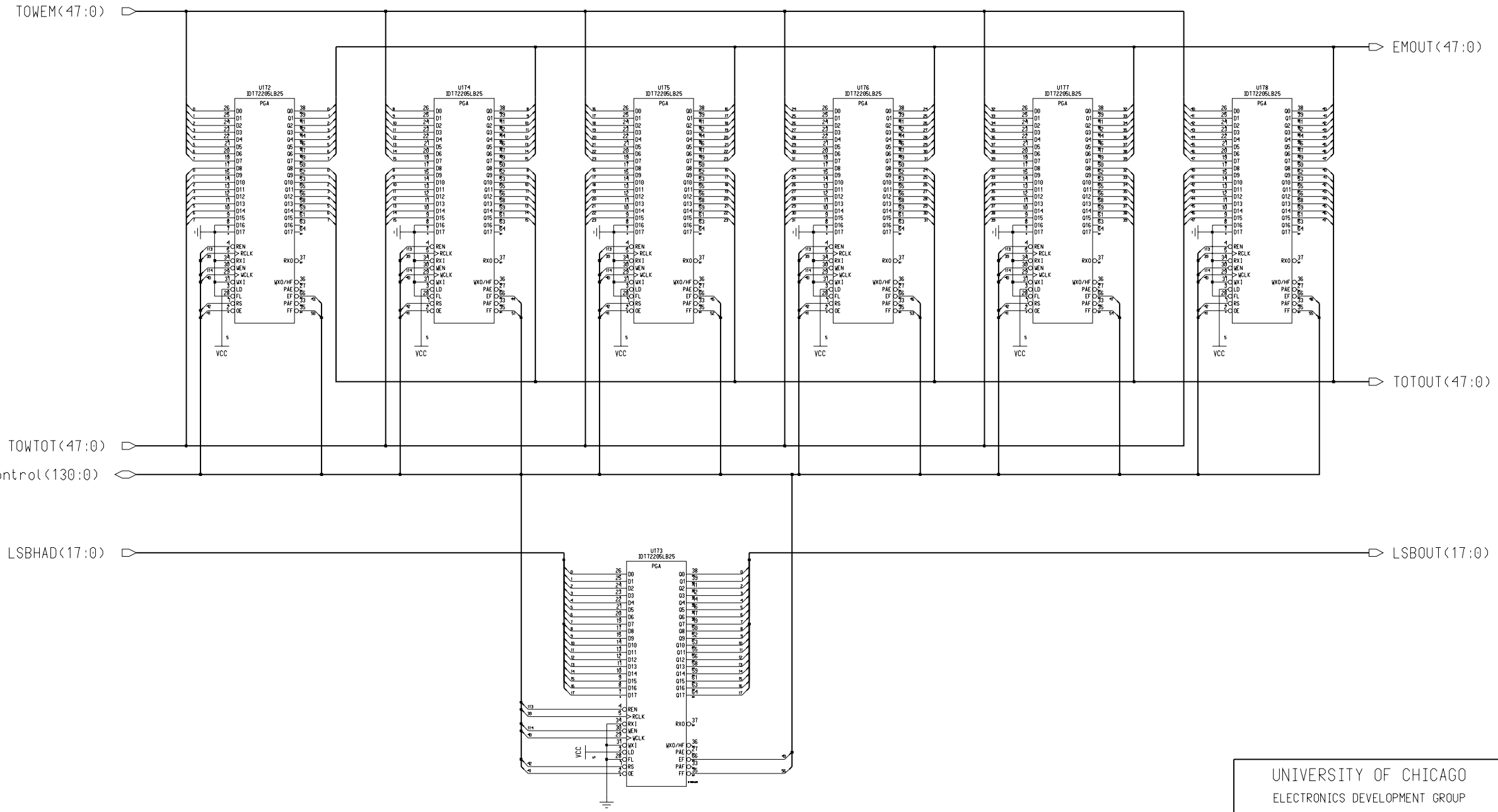
Control Signals

Control(39) - Read Clock/SO
Control(40) - Write clock/SI
Control(41) - Output Enable*
Control(42) - Reset*
Control(49:43) - Empty Flag*
Control(56:50) - Full Flag*
Control(113) - FIFO REN*
Control(114) - FIFO WEN*



DATE	REVISION DESCRIPTION
20 June 1995	Second Prototype: Merely a small change in the width of the data being aligned
18 Nov 1996	3rd Prototype - Bug Fixes

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
DIRAC / AL FIFO

SHEET 16 OF 24
DATE 18 Nov 1996
DRWN JW

C-2351
REV C