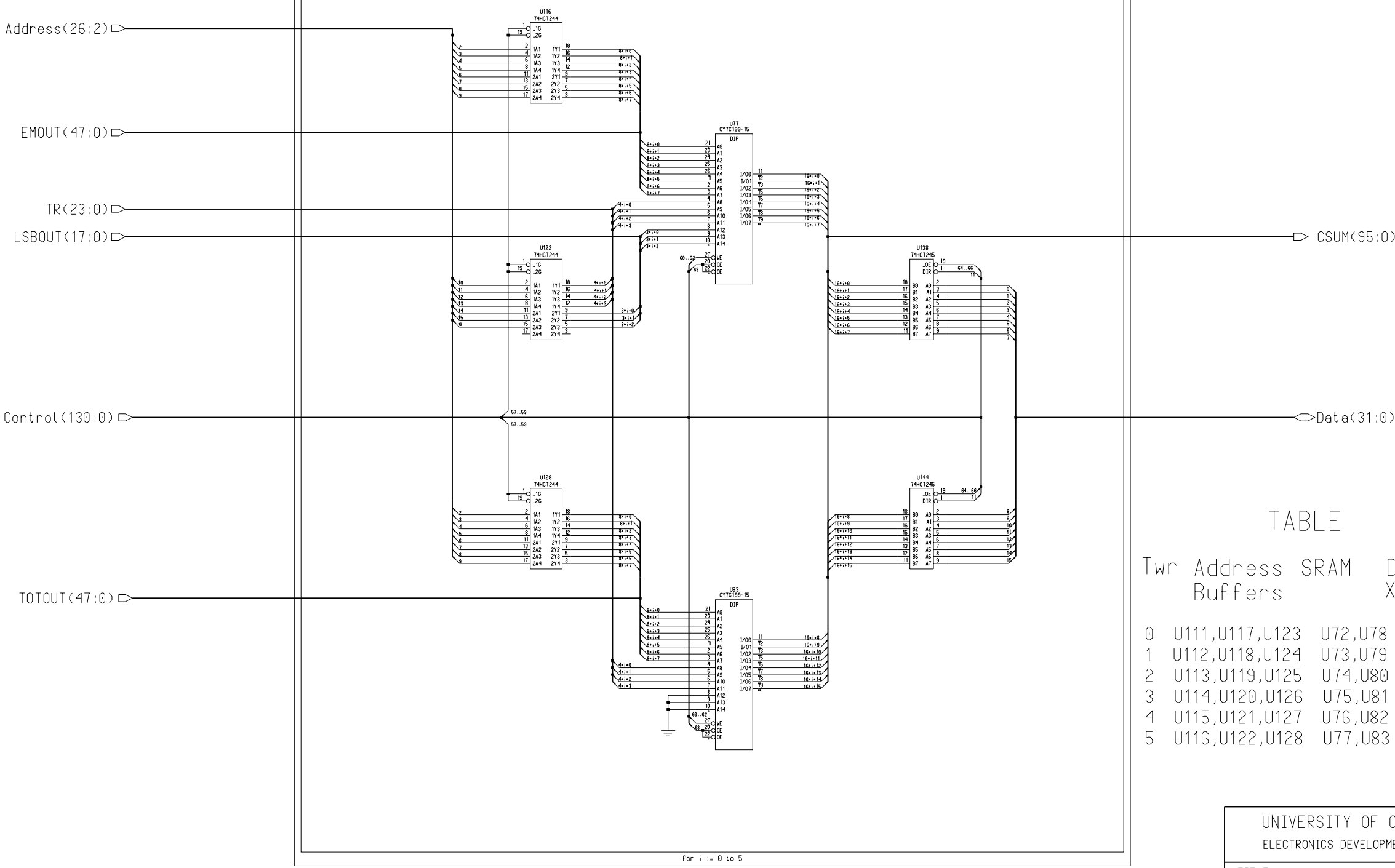
Control Signals

Control(59:57) - Address Access to TT MLU*
Control(62:60) - Write Enable for TT MLU*
Control(63) - Chip Enable and OE for TT MLU*
Control(66:64) - Data Access to TT MLU*
Control(11) - Write



TABLE

Twr	Address Buffers	SRAM	Data Xceivers
0	U111,U117,U123	U72,U78	U133,U139
1	U112,U118,U124	U73,U79	U134,U140
2	U113,U119,U125	U74,U80	U135,U141
3	U114,U120,U126	U75,U81	U136,U142
4	U115,U121,U127	U76,U82	U137,U143
5	U116,U122,U128	U77,U83	U138,U144

DATE	REVISION DESCRIPTION
20 June 1995	Second Prototype: Up to 32kX9 SRAMs for Had over EM
23 April 1998	3rd Prototype - Bug Fixes

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
DIRAC / Decision

SHEET 17 OF 24
DATE 18 Nov 1996
DRWN JW / MB

C-2351
REV C