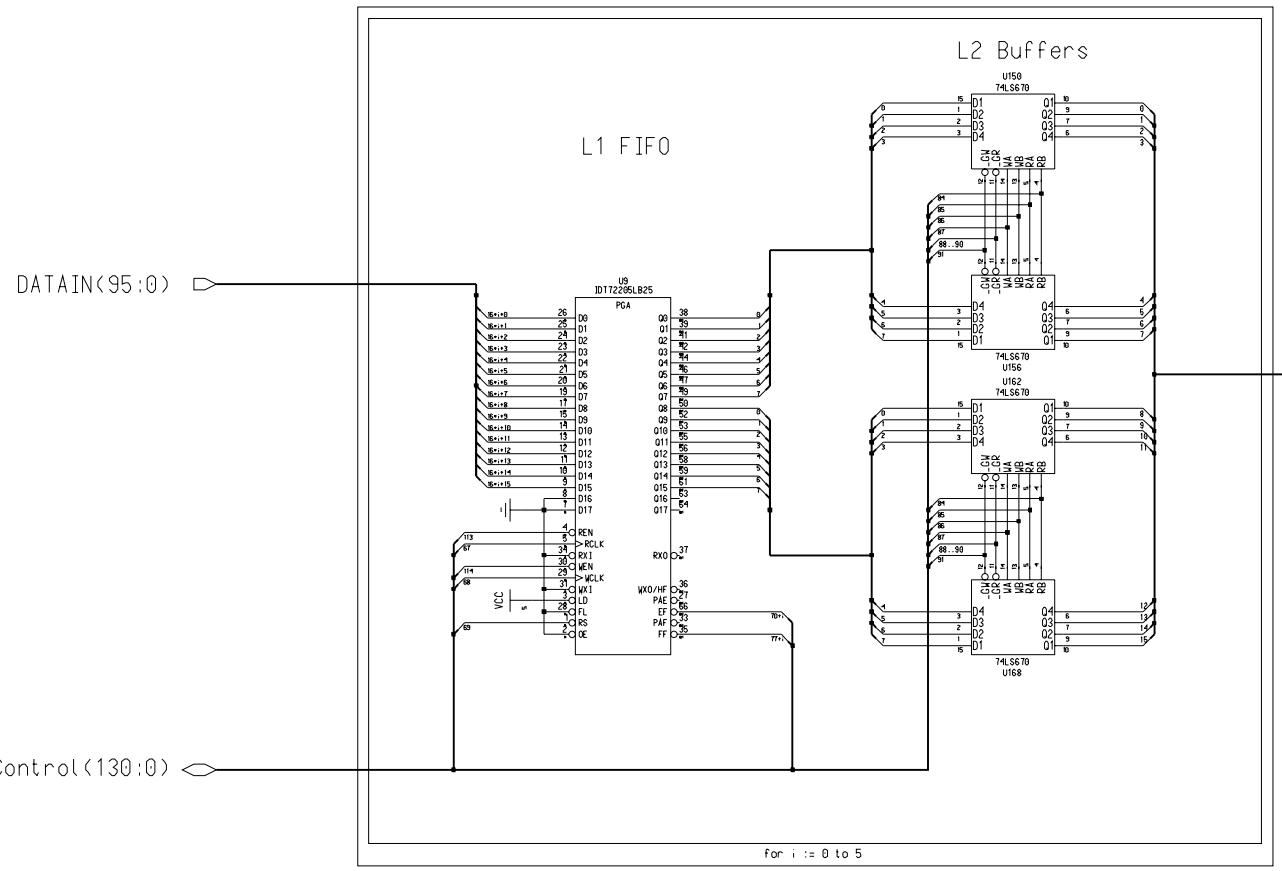

Control Signals

Control(67)	- Read Clock/SO
Control(68)	- Write Clock/SI
Control(69)	- Reset*
Control(75:70)	- Empty Flag*
Control(82:77)	- Full Flag*
Control(84)	- Read Address B
Control(85)	- Read Address A
Control(86)	- Write Address B
Control(87)	- Write Address A
Control(90:88)	- Enable Read*
Control(91)	- Write Enable*
Control(113)	- FIFO REN*
Control(114)	- FIFO WEN*

TABLE

Tower	L1 FIFO	L2 Buffers
0	U4	U157,U163,U145,U151
1	U5	U158,U164,U146,U152
2	U6	U159,U165,U147,U153
3	U7	U160,U166,U148,U154
4	U8	U161,U167,U149,U155
5	U9	U162,U168,U150,U156

DATE	REVISION DESCRIPTION
23 June 1995	Second Prototype: No change here.
18 Nov 1996	3rd Prototype - Bug Fixes

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
DIRAC / DAQ

SHEET 18 OF 24
DATE 18 Nov 1996
DRWN JW

C-2351
REV C