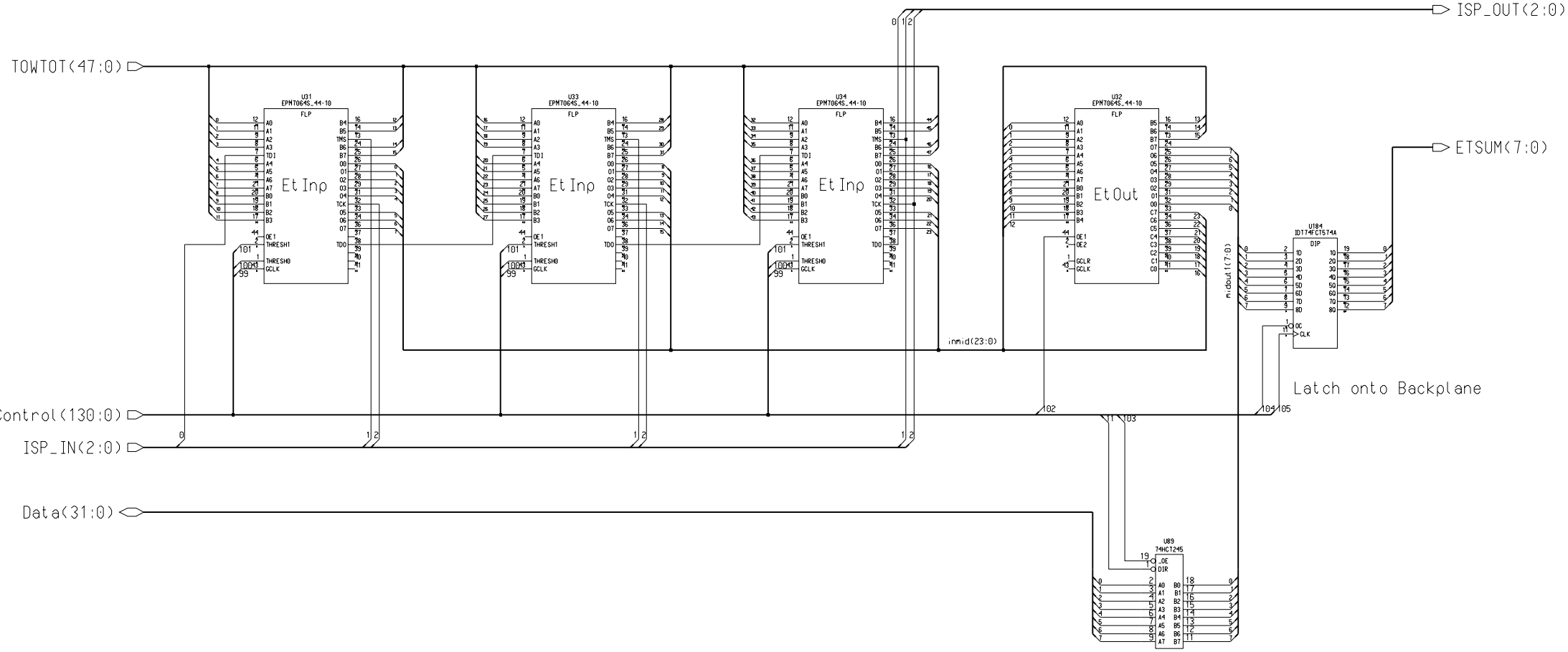

EtSum Controls

Control(99) - Latch EtSum In
Control(100) - Et Threshold(0)
Control(101) - Et Threshold(1)
Control(102) - Enable Outputs of ETOUT *
Control(103) - EnableEtSum Data Access*
Control(104) - Enable Outputs of BP Latch*
Control(105) - CLK for Data path onto BP
Control(11) - Write/DIR* for Transceiver

ISP INPUT
ISP_IN(0) - TDI From Previous Chip in Chain
ISP_IN(1) - TMS Signal
ISP_IN(2) - TCK Signal

ISP OUTPUT
ISP_OUT(0) - TDO To Next Chip in Chain
ISP_OUT(1) - TMS Signal(Tied to ISP_IN(1))
ISP_OUT(2) - TCK Signal(Tied to ISP_IN(2))

DATE	REVISION DESCRIPTION
28 June 1995	Second Prototype: Minor changes to incorporate the sum in TOWLAT.
18 Nov 1996	3rd Prototype - Bug Fixes

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
DIRAC / EtSum

SHEET 21 OF 24
DATE 18 Nov 1996
DRWN JW

C-2351
REV C