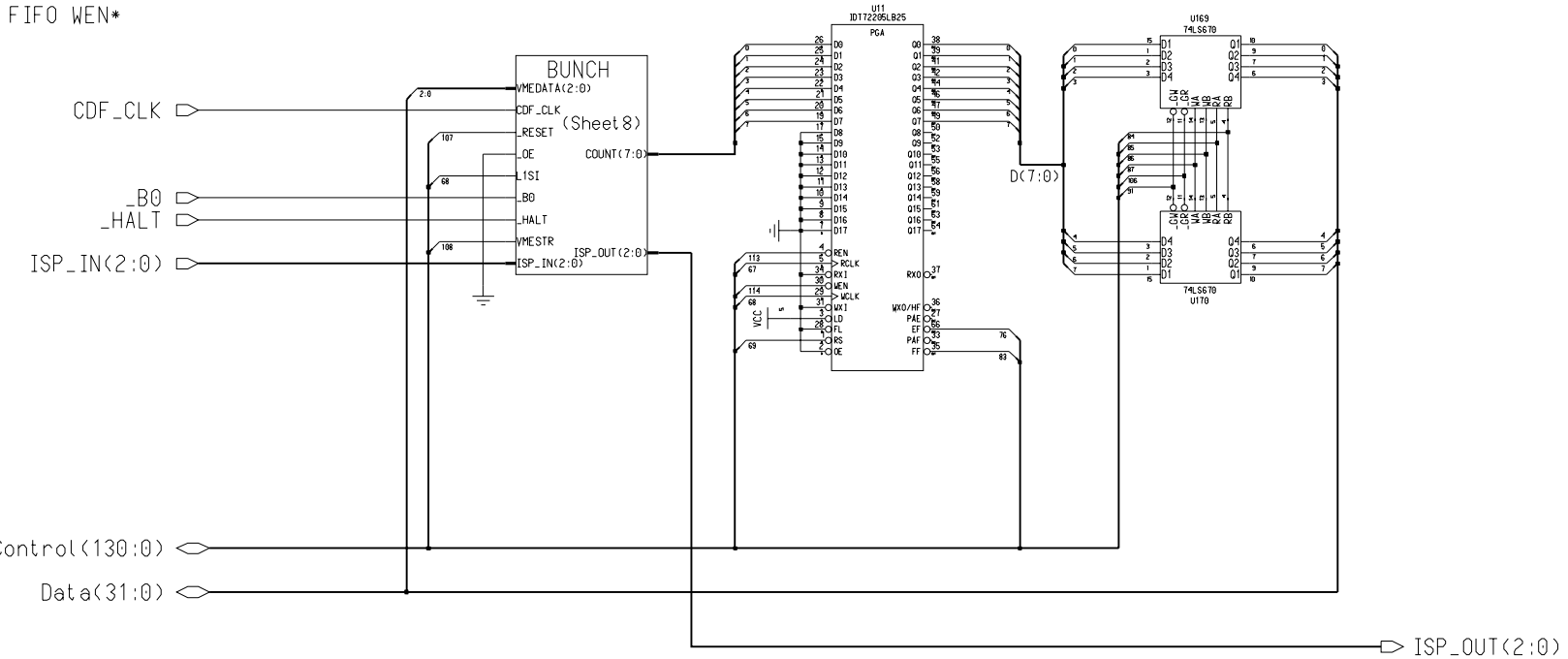
Bunch Counter Controls

Control(106) - Enable Read for L2Buf*
Control(107) - Reset for Bunch Counter*
Control(108) - VME Strobe for Bunch Counter
Control(67) - Read Clock/SO
Control(68) - Write Clock/SI
Control(69) - Reset*
Control(76) - Empty Flag*
Control(83) - Full Flag*
Control(84) - Read Address B
Control(85) - Read Address A
Control(86) - Write Address B
Control(87) - Write Address A
Control(91) - Write Enable*
Control(113) - FIFO REN*
Control(114) - FIFO WEN*



ISP INPUT
ISP_IN(0) - TDI From Previous Chip in Chain
ISP_IN(1) - TMS Signal
ISP_IN(2) - TCK Signal

ISP OUTPUT
ISP_OUT(0) - TDO To Next Chip in Chain
ISP_OUT(1) - TMS Signal(Tied to ISP_IN(1))
ISP_OUT(2) - TCK Signal(Tied to ISP_IN(2))

DATE	REVISION DESCRIPTION
14 Dec 1995	Original design - JW
23 April 1998	3rd Prototype - Bug Fixes

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
DIRAC / Bunch Counter

SHEET 7 OF 24
DATE 18 Nov 1996
DRWN JW

C-2351
REV C