Specification of Transition Module for Autonomous inputs to PreFRED

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This note specifies a VME transition module to allow single NIM, ECL, TTL or LVDS signals to be brought to a PreFRED module for the L1 Trigger. The purpose is to allow special input from scintillators, luminosity counters etc to be easily incorporated into the L1 system. This is an important function that gives CDF II more flexibility and room to evolve than it had before.

The form of the module is a simplified version of the existing L1AUX card used with DIRAC and PreFRED modules.

Mechanical:

- Board dimensions: 9Ux400mm Eurocard following IEE 1101.11 specs
- Board thickness: 0.093"
- P0 connector: (95 pin 2mm Hard Metric) for power connections
- P2 connector: not required but the foot print will be provided to mount a connector shell for alignment
- P3 connector: 220pin 2mm Hard Metric for output to PreFRED
- A board stiffener will be installed as close to the backplane connectors as feasible. This will be of the type described by Fermilab drawing: Drawing WS-9USTIF-032597.

Inputs:

- 30 single bit inputs divided up by logic level
- 4 single ended NIM Channels (channels 0-3)
- 2 single ended TTL channels (channels 4-5)
- 2 single ended ECL channels (channels 6-7)

- 2 differential LVDS channels (channels 8-9)
- 20 differential LVDS channels on two standard L1 input connectors (channels 10-29)

Input Connectors:

- Channels 0-5: NIM and TTL use LEMO type coaxial connectors, preferably a right angle board mount.
- Channels 6-9: LVDS and ECL use LEMO Differential connector, right angle board mount. LEMO P/N EPG.0B.302.HLN board mount.
- Channels 10-29: use the standard L1 input connector, Fujitsu FCN235D020-G/E

Connector shield connections:

- Connector shields do not connect directly to board ground.
- Allowance for AC connection to board ground should be made in the same fashion as the standard L1AUX card.
- Connector sheilds must not make electrical contact to the board front panel. This is most easily accomplished through the use of a on conductive panel as is done with the standard L1AUX card.

Outputs:

- 16 single ended TTL
- Connector 220 pin HM connector in VME J3 position
- Pinout of J3 connector given in Table 1

Power

- +5V xxmA from P0 connector (pins a1, b1, c1, d1, e1, c2)
- -5.2V yy mA from P0 connector (pins a4, a5, a9, a10, a11, a12, a16, a17)
- There will be a panel indicator for each voltage
- Power supplies will be fused and have transient suppressors

Table 1: J3 connector pin assignments for the Autonomous PreFRED Transition module. **TRIGBIT** = output trigger bits to FRED, these are No Connects on the transition module. **IN**(**x**) = Input: 0-3 correspond to single bit input NIM, 4-5 correspond to single bit input ECL, 6-7 correspond to single bit input ECL, 8-9 correspond to single bit input LVDS, 10-19 correspond to 10 channels on one L1 connector and 20-29 to 10 bits on the other L1 connector. **Not Used** means these are not provided by the transition these should be No Connects or grounded, whichever is better for the Altern chip on ProFRED.

| | Connects or grounded, whichever is better for the Altera chip on PreFRED. | | | | | | | | |
|--|---|-----|-----|---------------------------------------|----------------------|----------------------|----------------------|-----|--|
| Carlo Carl | | Row | | | | | | | |
| 2 | Pin # | | | | | | | | |
| 3 | | | | | | | | | |
| 4 | | | | | | | | | |
| S | | | | TRIGBIT(7) | | | | | |
| 6 | | | | | | | | | |
| 7 | | | | TRIGBIT(13) | | TRIGBIT(14) | TRIGBIT(15) | | |
| S | | | | | | | | | |
| 9 | | GND | N/C | GND | GND | GND | GND | GND | |
| 10 | | GND | N/C | GND | GND | GND | NIM2 | GND | |
| 11 | 9 | GND | GND | GND | GND | GND | GND | | |
| 12 | 10 | GND | N/C | GND | GND | GND | GND | GND | |
| 13 | 11 | GND | N/C | GND | GND | GND | NIM3 | GND | |
| 14 | 12 | GND | N/C | GND | GND | GND | GND | GND | |
| 15 | 13 | GND | GND | GND | GND | GND | GND | GND | |
| 15 | 14 | GND | N/C | GND | GND | NIM4 | GND | GND | |
| 16 | 15 | GND | | GND | GND | GND | GND | GND | |
| 17 | 16 | GND | | GND | GND | GND | GND | GND | |
| 18 | 17 | GND | | GND | GND | $\mathrm{TTL}1$ | GND | GND | |
| 19 | 18 | | N/C | GND | GND | GND | GND | | |
| Cond | | | | | GND | GND | GND | | |
| Carre Carr | 20 | GND | | GND | $\mathrm{TTL}2$ | GND | GND | GND | |
| 22 GND N/C GND GND GND GND 23 GND N/C ECL1 GND GND GND GND 24 GND N/C GND GND GND GND GND 25 GND GND GND GND GND GND GND 26 GND N/C ECL2 GND GND GND GND 27 GND N/C GND GND GND GND GND 28 GND N/C GND GND GND GND GND 29 GND GND GND GND GND GND GND 30 GND N/C GND GND GND GND GND 31 GND N/C GND GND GND GND GND 32 GND N/C GND GND GND GND GND | | | | | | | | | |
| 23 GND N/C ECL1 GND GND GND GND 24 GND N/C GND GND GND GND GND GND 25 GND GND GND GND GND GND GND GND 26 GND N/C ECL2 GND GND GND GND GND 27 GND N/C GND < | 22 | | N/C | GND | GND | GND | GND | | |
| 24 GND N/C GND GND GND GND GND 25 GND GND GND GND GND GND GND 26 GND N/C ECL2 GND GND GND GND 27 GND N/C GND GND GND GND GND 28 GND N/C GND GND GND GND GND 29 GND GND GND GND GND GND GND 30 GND GND GND GND GND GND GND 31 GND N/C GND GND GND GND GND GND 32 GND N/C GND LVDS3(1) GND GND LVDS3 | 23 | | | ECL1 | GND | GND | GND | | |
| 25 | | | | | | | | | |
| 26 GND N/C ECL2 GND GND GND GND 27 GND N/C GND GND GND GND GND 28 GND N/C GND GND GND GND GND 29 GND GND GND GND GND GND GND 30 GND N/C GND GND GND GND GND 31 GND N/C GND GND GND GND GND 32 GND N/C GND GND GND GND GND 33 GND GND GND GND GND GND GND 34 GND N/C GND GND GND LVDS3(1) GND 35 GND N/C LVDS3(2) LVDS3(3) GND LVDS3(4) GND 36 GND N/C LVDS3(5) LVDS3(6) LVDS4(7) LV | 25 | | | GND | GND | GND | GND | | |
| Connector Key (equivalent to 3 pins) | | | N/C | | GND | | GND | | |
| 28 GND N/C GND GND GND LVDS1 GND 29 GND GND GND GND GND GND GND 30 GND N/C GND GND GND GND GND 31 GND N/C GND GND GND GND GND 32 GND N/C GND GND GND GND GND 33 GND GND GND GND GND GND GND 34 GND N/C GND GND LVDS3(0) LVDS3(1) GND 35 GND N/C LVDS3(2) LVDS3(3) GND LVDS3(4) GND 36 GND N/C LVDS3(5) LVDS3(6) LVDS3(7) LVDS3(8) GND 37 GND GND LVDS4(0) LVDS4(1) GND 38 GND N/C LVDS4(2) LVDS4(3) LVDS4(4) LVDS4(8) | | | | | | | | | |
| 29 GND GND GND GND GND GND GND 30 GND N/C GND GND GND GND GND GND 31 GND N/C GND GND GND LVDS2 GND 32 GND N/C GND GND GND GND GND GND 33 GND < | | | | | | | | | |
| 30 | | | | | | | | | |
| 31 GND N/C GND GND GND LVDS2 GND 32 GND N/C GND LVDS3(1) GND GND GND LVDS3(1) GND GND GND LVDS3(2) LVDS3(2) LVDS3(3) GND LVDS3(4) GND GND LVDS3(4) GND GND LVDS3(8) GND GND LVDS3(8) GND GND LVDS4(1) GND GND LVDS4(1) GND GND LVDS4(1) GND GND LVDS4(1) GND GND LVDS4(5) GND GND LVDS4(8) GND GND LVDS4(8) GND LVDS4(8) GND LVDS4(8) GND LVDS4(8) GND LVDS4(8) GND TRIGBIT(16) TRIGBIT(17) GND AUX <t< td=""><td>30</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<> | 30 | | | | | | | | |
| 32 GND N/C GND LVDS3(0) LVDS3(1) GND GND 35 GND LVDS3(2) LVDS3(3) GND LVDS3(4) GND 36 GND N/C LVDS3(2) LVDS3(3) GND LVDS3(4) GND GND AUDS3(8) GND AUDS3(| 31 | | | | GND | | LVDS2 | | |
| Samp | 32 | | | GND | GND | | GND | | |
| 34 GND N/C GND GND LVDS3(0) LVDS3(1) GND 35 GND N/C LVDS3(2) LVDS3(3) GND LVDS3(4) GND 36 GND N/C LVDS3(5) LVDS3(6) LVDS3(7) LVDS3(8) GND 37 GND GND LVDS4(0) LVDS4(1) GND 38 GND N/C LVDS4(2) LVDS4(3) LVDS4(4) LVDS4(5) GND 39 GND N/C LVDS4(6) LVDS4(4) GND LVDS4(8) GND 40 GND N/C LVDS4(9) N/C TRIGBIT(16) TRIGBIT(17) GND 41 GND GND TRIGBIT(18) N/C TRIGBIT(19) B0_DELAYED GND 42 GND N/C BP_SPARE(1) GND BP_SPARE(2) GND 43 GND N/C AUX_ENABLE N/C N/C N/C GND | 33 | | | GND | GND | GND | GND | GND | |
| 35 GND N/C LVDS3(2) LVDS3(3) GND LVDS3(4) GND 36 GND N/C LVDS3(5) LVDS3(6) LVDS3(7) LVDS3(8) GND 37 GND GND LVDS4(0) LVDS4(1) GND 38 GND N/C LVDS4(2) LVDS4(3) LVDS4(4) LVDS4(5) GND 39 GND N/C LVDS4(6) LVDS4(4) GND LVDS4(8) GND 40 GND N/C LVDS4(9) N/C TRIGBIT(16) TRIGBIT(17) GND 41 GND GND TRIGBIT(18) N/C TRIGBIT(19) B0_DELAYED GND 42 GND N/C BP_SPARE(1) GND BP_SPARE(2) GND 43 GND N/C AUX_ENABLE N/C N/C N/C GND | | | | | | | | | |
| 35 GND N/C LVDS3(2) LVDS3(3) GND LVDS3(4) GND 36 GND N/C LVDS3(5) LVDS3(6) LVDS3(7) LVDS3(8) GND 37 GND GND LVDS4(0) LVDS4(1) GND 38 GND N/C LVDS4(2) LVDS4(3) LVDS4(4) LVDS4(5) GND 39 GND N/C LVDS4(6) LVDS4(4) GND LVDS4(8) GND 40 GND N/C LVDS4(9) N/C TRIGBIT(16) TRIGBIT(17) GND 41 GND GND TRIGBIT(18) N/C TRIGBIT(19) B0_DELAYED GND 42 GND N/C BP_SPARE(1) GND BP_SPARE(2) GND 43 GND N/C N/C N/C N/C N/C GND | 34 | GND | N/C | | • • • | | LVDS3(1) | GND | |
| 36 GND N/C LVDS3(5) LVDS3(6) LVDS3(7) LVDS3(8) GND 37 GND GND LVDS4(0) LVDS4(1) GND 38 GND N/C LVDS4(2) LVDS4(3) LVDS4(4) LVDS4(5) GND 39 GND N/C LVDS4(6) LVDS4(4) GND LVDS4(8) GND 40 GND N/C LVDS4(9) N/C TRIGBIT(16) TRIGBIT(17) GND 41 GND GND TRIGBIT(18) N/C TRIGBIT(19) B0_DELAYED GND 42 GND N/C BP_SPARE(1) GND BP_SPARE(2) GND 43 GND N/C N/C N/C N/C N/C GND | | | | | | | \ / | GND | |
| 37 GND GND LVDS3(9) GND LVDS4(0) LVDS4(1) GND 38 GND N/C LVDS4(2) LVDS4(3) LVDS4(4) LVDS4(5) GND 39 GND N/C LVDS4(6) LVDS4(4) GND LVDS4(8) GND 40 GND N/C LVDS4(9) N/C TRIGBIT(16) TRIGBIT(17) GND 41 GND GND TRIGBIT(18) N/C TRIGBIT(19) B0_DELAYED GND 42 GND N/C BP_SPARE(1) GND BP_SPARE(2) GND 43 GND N/C N/C N/C N/C N/C GND | | | | , , , | | | | | |
| 38 GND N/C LVDS4(2) LVDS4(3) LVDS4(4) LVDS4(5) GND 39 GND N/C LVDS4(6) LVDS4(4) GND LVDS4(8) GND 40 GND N/C LVDS4(9) N/C TRIGBIT(16) TRIGBIT(17) GND 41 GND GND TRIGBIT(18) N/C TRIGBIT(19) B0_DELAYED GND 42 GND N/C BP_SPARE(1) GND BP_SPARE(2) GND 43 GND N/C N/C N/C N/C GND | | | | | | | | | |
| 39 | | | | | LVDS4(3) | ` ' | \ / | | |
| 40 GND N/C LVDS4(9) N/C TRIGBIT(16) TRIGBIT(17) GND 41 GND GND TRIGBIT(18) N/C TRIGBIT(19) B0_DELAYED GND 42 GND N/C BP_SPARE(0) BP_SPARE(1) GND BP_SPARE(2) GND 43 GND N/C N/C N/C GND | | | | | | | \ / | | |
| 41 GND GND TRIGBIT(18) N/C TRIGBIT(19) B0_DELAYED GND 42 GND N/C BP_SPARE(0) BP_SPARE(1) GND BP_SPARE(2) GND GND N/C N/C GND G | | | | \ / | | | | | |
| 42 GND N/C BP_SPARE(0) BP_SPARE(1) GND BP_SPARE(2) GND | | | | | | | | | |
| 43 GND N/C N/C AUX_ENABLE N/C N/C GND | | | | | | ` ' | | | |
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