



- Comp. Side
- Layer Order
- 1.Signal\_1 Microstrip
  - 2.Power: +3.3V, +5V<sub>an</sub>
  - 3.Signal\_2 Stripline
  - 4.Power: DGND, AGND
  - 5.Signal\_3
  - 6.
  - 7.
  - 8.Signal\_4
  - 9.Power: DGND, AGND
  - 10.Signal\_5
  - 11.Power: -5V<sub>an</sub>
  - 12.Signal\_6

Board Characteristics

0. All dimensions are given in inches unless specified otherwise.
1. Material FR4 with Tg>170C, E.g. FR406
- 2.
3. Minimum trace width and clearance: 0.005".
4. 1 oz copper for all power layers and for Signal\_1,2 (Top and Bottom)  
1/2 oz copper for Stripline trace layers (Signal\_2,3,4,5).
5. Immersion Gold over copper, with min. Ni: 2.5-5 um; Au: 0.05-0.2 um.  
Apply Solder Mask over bare copper.
6. Board Thickness: 0.063 +/- 0.008
- 7.
8. Silkscreen on Component and Solder Sides.
9. 45 degree chamfer.
10. FHS tolerances: +/- 0.002 unless specified otherwise.
11. Interlayer spacing as specified
12. Zc=55 Ohm +/- 5 Ohm for 0.005" stripline and 0.006" microstrip traces on all layers.  
Perform TDR test for all signal layers.  
Present TDR test results for all signal layers.
13. Present plots for inspection before making boards.

BOARD'S DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
○	.014	3412	YES	---	
⊞	.041	553	YES	---	
⊕	.042	20	YES	---	
⊞	.057	10	YES	---	
⊖	.1023622	4	NO	---	
⊞	.106	6	NO	---	
⊕	.125	4	YES	---	
□	.16	4	YES	---	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XXX DO NOT SCALE DRAWING		CONTRACT NO.		UNIVERSITY OF CHICAGO ELECTRONICS DEVELOPMENT GROUP			
TREATMENT		APPROVALS	DATE	TITLE QUIET-PreAmp Board Specification Drawing			
FINISH		DRAWN M. Bogdan	9/1/06	SIZE B	FSCM NO.	DWG. NO. A - 2591	REV. A
SIMILAR TO		CHECKED M. Bogdan	9/1/06	ISSUED		SCALE 1/2	SHEET