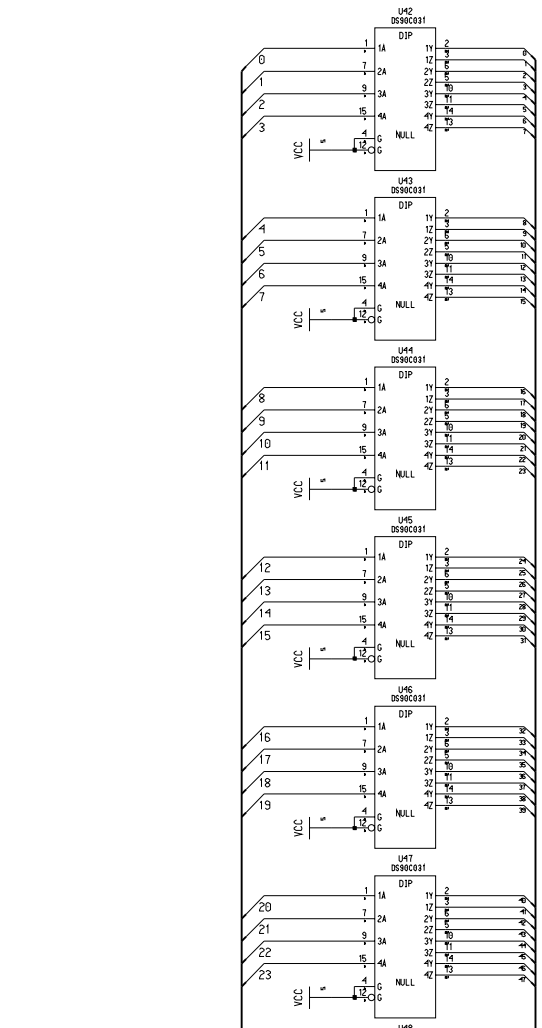
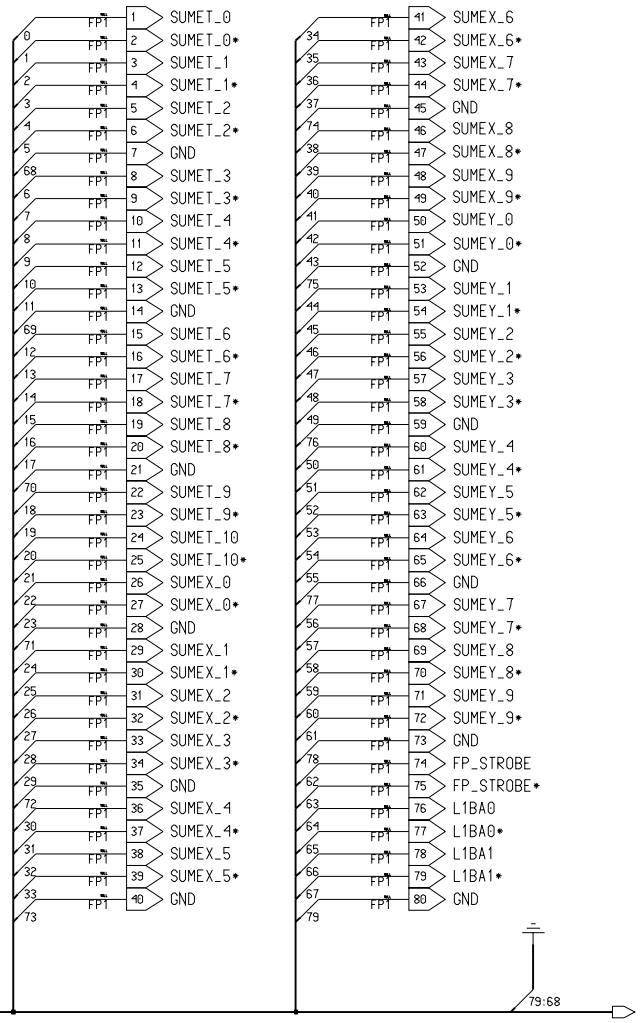


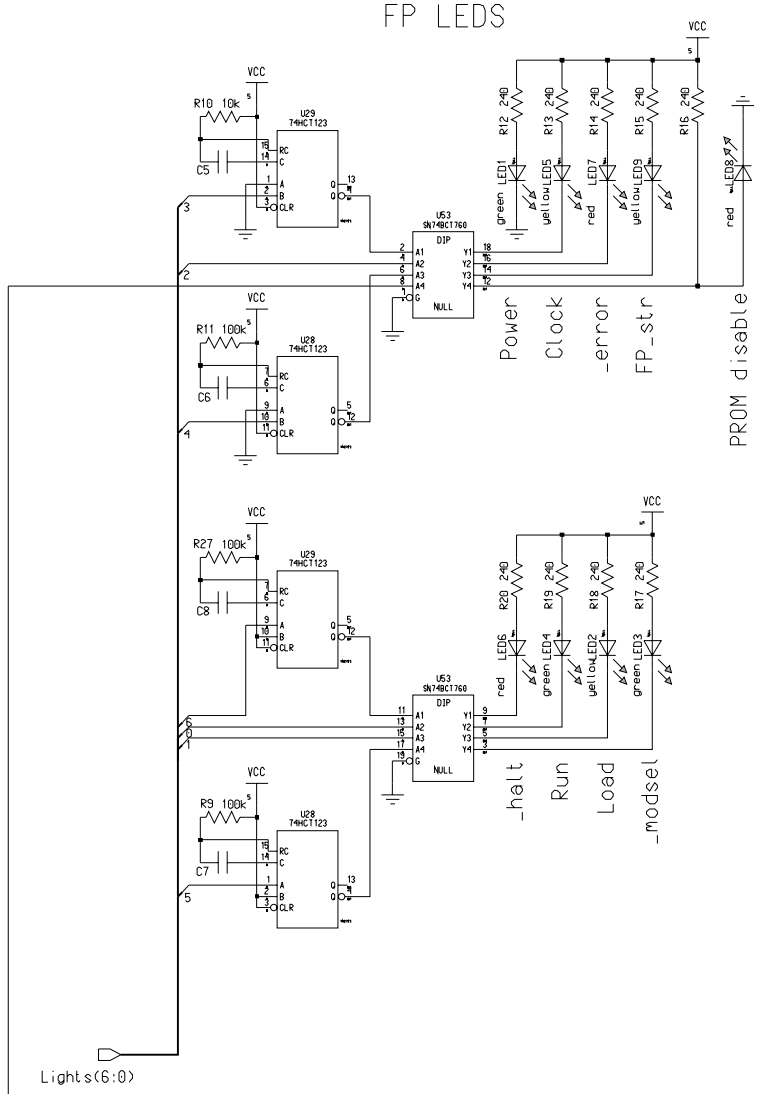
Append L1 buffer address to L2 data in order to tag the event

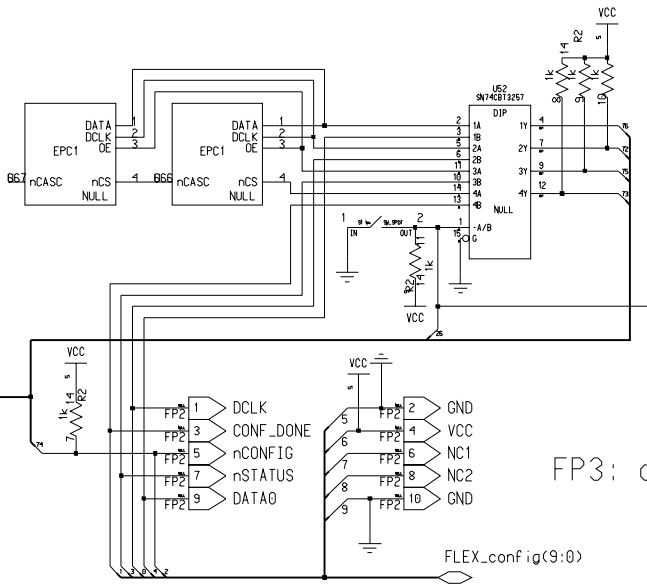
FP1: output to L2 processors

Note: FP1 is a 80-pin Honda connector

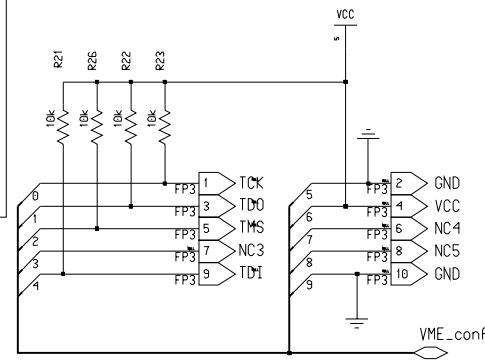


FP LEDS





FP2: connector to FLEX Download Cable



FP3: connector to VME_Interface Bit Blaster

FPanel controls

Control(14) - DAQ buffer read-address(0)

Control(15) - DAQ buffer read-address(1)

Control(28) - FP strobe validating data to L

DATE	REVISION DESCRIPTION
20 Feb 1997	PreFRED customization from original DIRAC
1 Oct 1997	Added FLEX Download Cable connector
May 12, 1999	Added R26(FP3/5toVCC), reconnected U41/1,7 Added R27, C8 and 74HCT123 on Lights(6)

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
PreFRED / Front Panel

SHEET 8 OF 13
DATE 20 Feb 1997
DRWN Alexis Amadon

C-2392
REV B