DWG. NO. B - 2487 SH REV. A

Layer Order

1. Signal_1
2. Power +5V
3. Signal_2
4. Signal_3
5. Power GND
6. Signal_4
7. Signal_5
8. Power +2.5V
9. Signal_6
10. Signal_7
11. Power +3.3V
12. Signal_8

DRILL SYMBOL	FHS	COUNT	PLATED	Tolerance	COMMENT
○	.016	1956	YES	---	
⊞	.018	4764	YES	---	
⦶	.0236	117	YES	Note 12.	Note 12.
⊟	.033	104	YES	---	
⊖	.035	456	YES	---	
◫	.041	1040	YES	---	
⊕	.052	10	YES	---	
□	.0551	16	NO	---	
	.057	14	YES	---	
	.09	2	NO	---	
	.095	4	YES	---	
	.106	19	NO	---	
	.1063	24	NO	---	
	.113	9	NO	---	
	.128	4	NO	---	
	.16	1	YES	---	

12-1. Finished plated hole size: 0.59 - 0.65 mm.
12-2. Drilled hole size: 0.7mm +/- 0.02mm
12-3. Thickness of thru hole plating: min. 25 µm Cu;
Ni: 2.5-5 µm; Au (chem plated): 0.05 - 0.2 µm.

Board Characteristics

0. All dimensions are given in inches unless specified otherwise.
1. Material FR4 Tg>170C.
2. Minimum trace width 0.006" on all layers.
3. Minimum clearence 0.006" on all layers.
4. 1 oz Cu for the power layers, 1/2 oz Cu for the trace layers.
5. Ni/Au (chem plated) over bare copper.
Apply Solder Mask over bare copper.
6. Board Thickness: 0.093 +/- 0.008
7. Mill the Top and Bottom of board on the solder side
to a thickness of 0.062" +/- 0.008.
8. Silkscreen on Component and Solder Sides.
9. 45 degree chamfer.
10. FHS tolerances: +/- 0.002 unless specified otherwise.
11. Interlayer spacing as specified
13. Impedance : 58 Ohm +/- 5 Ohm for 0.006" traces on all layers.
14. Perform TDR test using existing test-traces on board.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XXX
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

CONTRACT NO.

APPROVALS		DATE
DRAWN	M.Bogdan	7/26/02
CHECKED	H.Sanders	7/26/02
ISSUED		

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE CDF Level2 Pulsar Board
Specification Drawing

SIZE B | FSCM NO. | DWG. NO. B - 2502 | REV. A

SCALE 1/4 | SHEET

THIS SHEET IS COMPUTER GENERATED