Pin Name (1)	**652-Pin BGA**	**655-Pin PGA**	**672-Pin FineLine BGA**
MSEL0 (2)	U35	A23	N21
MSEL1 (2)	W35	C23	N20
nSTATUS (2)	AN17	AE41	AA13
nCONFIG (2)	W32	C25	P21
DCLK (2)	U3	BA23	N7
CONF_DONE (2)	AM17	AC47	AA12
INIT_DONE (3)	C16	AE7	J15
nCE (2)	U1	BE25	P6
nCEO (2)	C19	AC9	G14
nWS (4)	M1	BF14	P9
nRS (4)	N1	AY20	N10
nCS (4)	P2	BB20	M9
CS (4)	R2	BD20	T6
RDYnBSY (4)	A14	AH4	J14
CLKUSR (4)	C15	AH6	K14
DATA7 (4)	M6	BG13	M10
DATA6 (4)	L6	BB16	L8
DATA5 (4)	E7	BC3	F6
DATA4 (4)	B5	AR7	G9
DATA3 (4)	B7	AV4	F10
DATA2 (4)	A8	AP6	J12
DATA1 (4)	C13	AH8	K13
DATA0 (2), (5)	U4	BE23	N6
TDI (2)	W1	BG23	P7
TDO (2)	C17	AE1	G13
TCK (2)	AN19	AC45	AA14
TMS (2)	AM19	AD40	AA15
TRST (2)	D19	AD2	F14
Dedicated Inputs	B17, B19, AP17, AP19	AB4, AC5, AC43, AE43	F13, H14, Y13, Y14
Dedicated Clock Pins	U2, W34	H24, AY24	N8, P20
LOCK (6)	AB6	BG29	U6
CLK2 (7)	U2	AY24	N8
DEV_CLRn (3)	T6	AY22	R9
DEV_OE (3)	Y5	BF26	R8
VCCINT	A17, A19, D12, D24, E12, E24, F3, F35, G30, H1, H5, K31, L3, M30, N4, N35 R5, R34, U5, U34, W3, W31, W33, AA4, AA31, AC3, AC32, AE2, AE33, AG1, AH4, AH31, AH35, AK33, AL2, AL12, AL24, AM12, AM24, AR17, AR19	A3, A45, B24, C1, C11, C19, C29, C37, C47, D24, G47, L3, L45, N1, N47, W3, W45, AA1, AA47, AD4, AD44, AG1, AG47, AJ3, AJ45, AR1, AR47, AU3, AU45, AY8, BA1, BA47, BD24, BE1, BE11, BE19, BE29, BE37, BE47, BG3, BG45	A3, A24, B3, B8, B19, B24, C1, C2, C25, C26, D3, D24, K11, L10, L15, M13, M16, N2, N12, P15, P16, P24, P25, R11, R14, T12, T17, U9, U16, AC3, AC24, AD1, AD2, AD25, AD26, AE3, AE8, AE19, AE24, AF3, AF24
VCCIO	AL3, AL4, AL17, AL19, AL31, AL32, AM5, AN4, AN32, AN33, C4, C32, D5, D31, E3, E4, E17, E19, F30, F31, U6, U30, W6, W30,	E9, E15, E21, E27, E33, E39, G7, G41, J5, J43, R5, R43, AA5, AA43, AG5, AG43, AN5, AN43, AW5, AW43, BA7, BA41, BC9, BC15, BC21, BC27, BC33, BC39	A6, A13, A21, J10, K9, K16, L12, L17, M11, M14, N3, N15, N24, P12, R13, R16, T10, T15, U11, U18, V10, V17, AF6, AF13, AF21
VCC_CKLK (8)	W4	BD28	N11

Pin Name (1)	**652-Pin BGA**	**655-Pin PGA**	**672-Pin FineLine BGA**
GNDINT	A1, A18, A35, B1, B2, B18, B34, B35, C2, C3, C18, C33, C34, C35, D2, D3, D4, D17, D18, D32, D33, D34, E5, E6, E18, E30, E31, E32, E33, F18, V1, V2, V3, V4, V5, V6, V30, V31, V32, V33, V34, V35, AK18, AL5, AL6, AL18, AL30, AM18, AM2, AM3, AM4, AM31, AM32, AM33, AM34, AN1, AN2, AN3, AN18, AN34, AN35, AP1, AP2, AP18, AP34, AP35, AR1, AR18, AR35,	A47, B2, C13, C21, C27, C35, C45, D4, F24, J1, J47, N3, N45, R1, R47, W1, W47, AA3, AA45, AD6, AD8, AD42, AG3, AG45, AJ1, AJ47, AN1, AN47, AR3, AR45, AW1, AW47, BB24, BE3, BE13, BE21, BE27, BE35, BE45, BG1, BG47	A2, A8, A14, A19, A25, B1, B2, B6, B21, B25, B26, C3, C13, C24, D4, D23, H8, H19, J9, J18, K10, K17, L11, L13, L16, M12, M15, N1, N4, N13, N14, N25, N26, P1, P2, P3, P13, P14, P23, P26, R12, R15, T11, T16, U10, U17, V9, V18, W8, W19, AC4, AC23, AD3, AD13, AD24, AE1, AE2, AE6, AE21, AE25, AE26, AF2, AF8, AF14, AF19, AF25
GNDIO (9)	–	E7, E13, E19, E29, E35, E41, G5, G43, H40, N5, N43, W5, W43, AJ5, AJ43, AR5, AR43, AY40, BA5, BA43, BC7, BC13, BC19, BC29, BC35, BC41, BF46	–
GND_CKLK (8)	W2	BD26	P11
No Connect (N.C.)	–	–	A15, A16, B13, B14, B15, B16, C11, C12, C14, C15, C16, AD11, AD12, AD14, AD15, AD16, AE12, AE13, AE14, AE15, AF12, AF15,
Total User I/O Pins (10)	502	502	502

Notes:

(1) All pins that are not listed are user I/O pins.
(2) This pin is a dedicated pin; it is not available as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK remains high if a periodic clock stops clocking. The LOCK function is optional; if the LOCK output is not used, this pin is a user I/O pin.
(7) This pin drives the ClockLock and ClockBoost circuitry.
(8) This pin is the power or ground for the ClockLock and ClockBoost circuitry. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. VCC_CKLK has the same voltage specifications as the VCCINT and should be connected to a 2.5-V power supply. If the ClockLock or ClockBoost circuitry is not used, this power or ground pin should be connected to VCCINT or GNDINT, respectively.
(9) GNDIO and GNDINT are connected together in BGA packages.
(10) The user I/O pin count includes dedicated inputs, dedicated clock inputs, and all I/O pins.