

Dedicated Pin	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP (1), (2)	160-Pin PQFP
INPUT/GCLK1	83	89	87	139
INPUT/GCLRn	1	91	89	141
INPUT/OE1	84	90	88	140
INPUT/OE2/GCLK2	2	92	90	142
TDI (3)	14	6	4	9
TMS (3)	23	17	15	22
TCK (3)	62	64	62	99
TDO (3)	71	75	73	112
GNDINT	42, 82	40, 88	38, 86	60, 138
GNDIO	7, 19, 32, 47, 59, 72	13, 28, 45, 61, 76, 97	11, 26, 43, 59, 74, 95	17, 42, 66, 95, 113, 148
VCCINT (5.0 V only)	3, 43	41, 93	39, 91	61, 143
VCCIO (3.3 V or 5.0 V)	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84	3, 18, 34, 51, 66, 82	8, 26, 55, 79, 104, 133
No Connect (N.C.)	—	—	—	1, 2, 3, 4, 5, 6, 7, 34, 35, 36, 37, 38, 39, 40, 44, 45, 46, 47, 74, 75, 76, 77, 81, 82, 83, 84, 85, 86, 87, 114, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157
Total User I/O Pins (4)	68	84	84	100

LAB	MC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP (1), (2)	160-Pin PQFP
A	1	–	4	2	160
A	2	–	–	–	–
A	3	12	3	1	159
A	4	–	–	–	158
A	5	11	2	100	153
A	6	10	1	99	152
A	7	–	–	–	–
A	8	9	100	98	151
A	9	–	99	97	150
A	10	–	–	–	–
A	11	8	98	96	149
A	12	–	–	–	147
A	13	6	96	94	146
A	14	5	95	93	145
A	15	–	–	–	–
A	16	4	94	92	144
B	17	22	16	14	21
B	18	–	–	–	–
B	19	21	15	13	20
B	20	–	–	–	19
B	21	20	14	12	18
B	22	–	12	10	16
B	23	–	–	–	–
B	24	18	11	9	15
B	25	17	10	8	14
B	26	–	–	–	–
B	27	16	9	7	13
B	28	–	–	–	12
B	29	15	8	6	11
B	30	–	7	5	10
B	31	–	–	–	–
B	32	14 (3)	6 (3)	4 (3)	9 (3)
C	33	–	27	25	41
C	34	–	–	–	–
C	35	31	26	24	33
C	36	–	–	–	32
C	37	30	25	23	31
C	38	29	24	22	30
C	39	–	–	–	–
C	40	28	23	21	29
C	41	–	22	20	28
C	42	–	–	–	–
C	43	27	21	19	27
C	44	–	–	–	25
C	45	25	19	17	24
C	46	24	18	16	23
C	47	–	–	–	–
C	48	23 (3)	17 (3)	15 (3)	22 (3)

LAB	MC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP (1), (2)	160-Pin PQFP
D	49	41	39	37	59
D	50	–	–	–	–
D	51	40	38	36	58
D	52	–	–	–	57
D	53	39	37	35	56
D	54	–	35	33	54
D	55	–	–	–	–
D	56	37	34	32	53
D	57	36	33	31	52
D	58	–	–	–	–
D	59	35	32	30	51
D	60	–	–	–	50
D	61	34	31	29	49
D	62	–	30	28	48
D	63	–	–	–	–
D	64	33	29	27	43
E	65	44	42	40	62
E	66	–	–	–	–
E	67	45	43	41	63
E	68	–	–	–	64
E	69	46	44	42	65
E	70	–	46	44	67
E	71	–	–	–	–
E	72	48	47	45	68
E	73	49	48	46	69
E	74	–	–	–	–
E	75	50	49	47	70
E	76	–	–	–	71
E	77	51	50	48	72
E	78	–	51	49	73
E	79	–	–	–	–
E	80	52	52	50	78
F	81	–	54	52	80
F	82	–	–	–	–
F	83	54	55	53	88
F	84	–	–	–	89
F	85	55	56	54	90
F	86	56	57	55	91
F	87	–	–	–	–
F	88	57	58	56	92
F	89	–	59	57	93
F	90	–	–	–	–
F	91	58	60	58	94
F	92	–	–	–	96
F	93	60	62	60	97
F	94	61	63	61	98
F	95	–	–	–	–
F	96	62 (3)	64 (3)	62 (3)	99 (3)

LAB	MC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP (1), (2)	160-Pin PQFP
G	97	63	65	63	100
G	98	–	–	–	–
G	99	64	66	64	101
G	100	–	–	–	102
G	101	65	67	65	103
G	102	–	69	67	105
G	103	–	–	–	–
G	104	67	70	68	106
G	105	68	71	69	107
G	106	–	–	–	–
G	107	69	72	70	108
G	108	–	–	–	109
G	109	70	73	71	110
G	110	–	74	72	111
G	111	–	–	–	–
G	112	71 (3)	75 (3)	73 (3)	112 (3)
H	113	–	77	75	121
H	114	–	–	–	–
H	115	73	78	76	122
H	116	–	–	–	123
H	117	74	79	77	128
H	118	75	80	78	129
H	119	–	–	–	–
H	120	76	81	79	130
H	121	–	82	80	131
H	122	–	–	–	–
H	123	77	83	81	132
H	124	–	–	–	134
H	125	79	85	83	135
H	126	80	86	84	136
H	127	–	–	–	–
H	128	81	87	85	137

Notes:

- (1) A complete thermal analysis should be performed before committing a design to this device package.
- (2) EPM7128E devices are not available in the 100-pin TQFP package.
- (3) This JTAG pin applies to MAX 7000S devices only and this pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for boundary-scan testing or for ISP, this pin is not available as a user I/O pin.
- (4) The user I/O pin count includes dedicated input pins and all I/O pins.

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