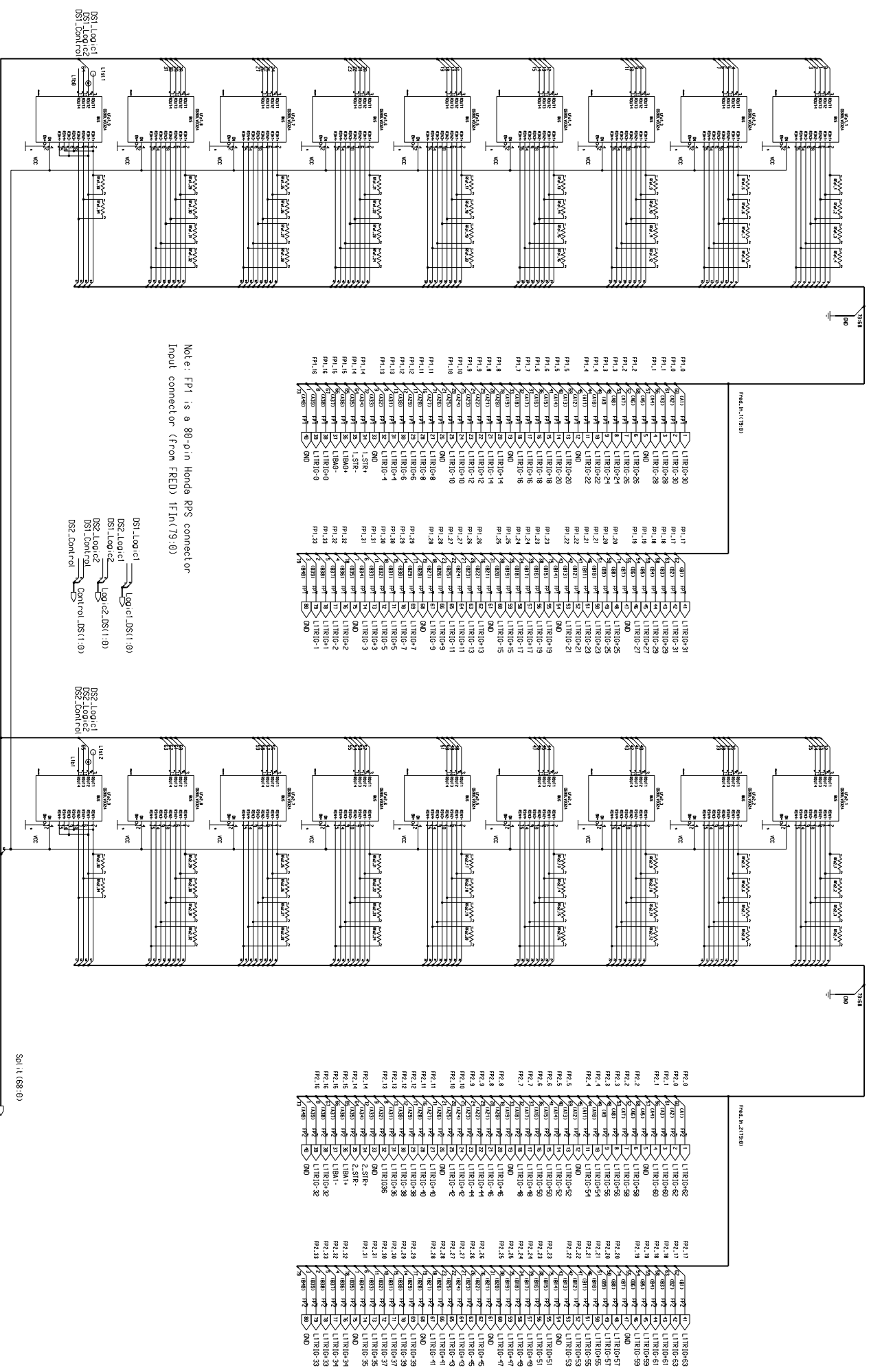


The L1 input signal map is based on Fred inputs on the interface board side. Note that the L1 output connector pin map is based on Fred signals on the Fred side. Need to remap the signals in firmware for Prefred signals.

the 64 L1 trigger bits are sent into FPGA as L1_IN(63:0), while L1Buffer bits (1:0) are L1_IN(65:64), and strobe 2 and 1 are L1_IN(67:66), and L1_IN(68) is the enable bit.



DATE	REVISION DESCRIPTION
2005-03-01	Completed the signal mapping (mbl/1)
2005-03-01	Added extra strobes.
2005-03-01	

UNIVERSITY OF CHICAGO
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TITLE **Pulsar**
Level 1 Inputs

SHEET 13 OF 25
DATE 2005-03-01
REV A