5-row P3 connector map to one SLINK LDC and one LSC (use P2-type backplane).
the signals into control FPGA are mapped in such a way to be consistent with the mezzanine card connector, to make life easier in firmware

The 32 data bits are mapped to S_IO(31:0), other signals are mapped to higher bits. the mapping is similar for both LDC and LSC signals.

P3

S2_IO(45:0)

LD3	Z1	129	3	LD2	A1	1	2	+3.3V	B1	33		LD1	C1	65	1
ground	Z2	130		LD5	A2	2	5	ground	B2	34		ground	C2	66	
LD7	Z3	131	7	ground	A3	3		P3_not_used1	B3	35		LD6	C3	67	6
ground	Z4	132		LD10	A4	4	10	P3_not_used2	B4	36	0	LD9	C4	68	9
LD14	Z5	133	14	LD13	A5	5	13	P3_not_used3	B5	37	1	LD12	C5	69	12
ground	Z6	134		LD17	A6	6	17	P3_not_used4	B6	38	2	LD16	C6	70	16
LD20	Z7	135	20	LD19	A7	7	19	P3_not_used5	B7	39	3	ground	C7	71	
ground	Z8	136		LD23	A8	8	23	P3_not_used6	B8	40	4	LD22	C8	72	22
LD25	Z9	137	25	ground	A9	9		P3_not_used7	B9	41	5	LD24	C9	73	24
ground	Z10	138		LD28	A10	10	28	P3_not_used8	B	42	6	LD27	C10	74	27
LCTRL#	Z11	139	33	LD31	A11	11	31	P3_not_used9	B11	43	7	LD30	C11	75	30
ground	Z12	140		LWEN#	A12	12	34	ground	B	44	8	ground	C12	76	
LCLK	Z13	141	32	ground	A13	13		+3.3V	B	45		UDW1_A	C13	77	38
ground	Z14	142		LDOWN#_A	A14	14	40	P3_not_used11	B	46		UXOFF#	C14	78	36
URL1	Z15	143	43	LDERR#	A15	15	41	P3_not_used12	B	47	9	URL0	C15	79	42
ground	Z16	144		URL3	A16	16	45	P3_not_used13	B	48	10	URL2	C16	80	44
UD3	Z17	145		UD2	A17	17		P3_not_used14	B	49	11	UD1	C17	81	
ground	Z18	146	3	UD5	A18	18	2	P3_not_used15	B	50	12	ground	C18	82	1
UD7	Z19	147		ground	A19	19	5	P3_not_used16	B	51	13	UD6	C19	83	
ground	Z20	148	7	UD10	A20	20		P3_not_used17	B	52	14	UD9	C20	84	6
UD14	Z21	149		UD13	A21	21	10	P3_not_used18	B21	53	15	UD12	C21	85	9
ground	Z22	150	14	UD17	A22	22	13	ground	B	54	16	UD16	C22	86	12
UD20	Z23	151		UD19	A23	23	17	P3_not_used19	B	55		ground	C23	87	16
ground	Z24	152	20	UD23	A24	24	19	P3_not_used20	B	56	17	UD22	C24	88	
UD25	Z25	153		ground	A25	25	23	P3_not_used21	B	57	18	UD24	C25	89	22
ground	Z26	154	25	UD28	A26	26		P3_not_used22	B	58	19	UD27	C26	90	24
UCTRL#	Z27	155		UD31	A27	27	28	P3_not_used23	B	59	20	UD30	C27	91	27
ground	Z28	156	33	UWEN#	A28	28	31	P3_not_used24	B	60	21	ground	C28	92	30
UCLK	Z29	157		ground	A29	29	34	P3_not_used25	B	61	22	UDW1_B	C29	93	
ground	Z30	158	32	LDOWN#_B	A30	30	40	P3_not_used26	B	62	23	LFF#	C30	94	38
LRL1	Z31	159		NC	A31	31	41	ground	B31	63	24	LRL0	C31	95	36
ground	Z32	160	43	LRL3	A32	32	45	+3.3V	B	64		LRL2	C32	96	42

LD0	D1	97	0												
LD4	D2	98	4												
ground	D3	99													
LD8	D4	100	8												
LD11	D5	101	11												
LD15	D6	102	15												
LD18	D7	103	18												
LD21	D8	104	21												
ground	D9	105													
LD26	D10	106	26												
LD29	D11	107	29												
UDW0_A	D12	108	37												
UTDO#	D13	109	39												
URESET#_A	D14	110	35												
ground	D15	111													
ground	D16	112													
UD0	D17	113													
UD4	D18	114	0												
ground	D19	115	4												
UD8	D20	116													
UD11	D21	117	8												
UD15	D22	118	11												
UD18	D23	119	15												
UD21	D24	120	18												
ground	D25	121	21												
UD26	D26	122													
UD29	D27	123	26												
UDW0_B	D28	124	29												
UTEST#	D29	125	37												
URESET#_B	D30	126	39												
ground	D31	127	35												
+3.3V	D32	128													

+3.3V

+3.3V

+3.3V

+3.3V

LDC SLOT C

LSC SLOT D

S1_IO(45:0)

S0_SP(24:0)

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
Level2 Pulsar / P3

DATE	REVISION DESCRIPTION

SHEET 14 OF 25
DATE 5/15/2002
DRWN MB/TL

C-2501
REV A