4. Stratix EP1S30 Device Pin Information

S5V3004-2.1

Introduction

The following tables contain pin information for the Stratix EP1S30 device, organized into the following sections:

Pin List

Table 4–1 shows the complete pin list for the EP1S30 device:

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 1 of 52)

Device					Package					
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA	DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
VCCINT					VCC	VCC	VCC			
VCCA_PLL7						L23	D31			
GND					GND	GND	GND			
GNDA_PLL7						M23	D32			
VCCG_PLL7						J23	D30			
GNDG_PLL7						K23	E30			
FPLL7CLKp			B2	VREF0B2		E31	L29			
FPLL7CLKn			B2	VREF0B2		D31	L28			
IO			B2	VREF0B2						
IO			B2	VREF0B2						
IO	DIFFIO_RX40p		B2	VREF0B2			E32			LOW
IO	DIFFIO_RX40n		B2	VREF0B2			E31			LOW
IO	DIFFIO_TX40p		B2	VREF0B2		K24	G25			HIGH
IO	DIFFIO_TX40n		B2	VREF0B2		J24	G26			HIGH
IO	DIFFIO_RX39p		B2	VREF0B2		F28	F29			HIGH
IO	DIFFIO_RX39n		B2	VREF0B2		G28	F30			HIGH
IO	DIFFIO_TX39p		B2	VREF0B2		K25	G28			HIGH
IO	DIFFIO_TX39n		B2	VREF0B2		J25	G27			HIGH
IO	DIFFIO_RX38p		B2	VREF0B2		J28	F31			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 2 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_RX38n		B2	VREF0B2		H28	F32			HIGH
IO	DIFFIO_TX38p		B2	VREF0B2	F24	H24	H28			HIGH
IO	DIFFIO_TX38n		B2	VREF0B2	F23	G24	H27			HIGH
VREF0B2			B2	VREF0B2	E24	L22	F27			
IO	DIFFIO_RX37p		B2	VREF0B2		D29	G29			HIGH
IO	DIFFIO_RX37n		B2	VREF0B2		E29	G30			HIGH
IO	DIFFIO_TX37p		B2	VREF0B2	G23	H25	J27			HIGH
IO	DIFFIO_TX37n		B2	VREF0B2	G24	G25	J28			HIGH
IO	DIFFIO_RX36p		B2	VREF0B2	C27	F29	H30			HIGH
IO	DIFFIO_RX36n		B2	VREF0B2	C28	G29	H29			HIGH
IO	DIFFIO_TX36p		B2	VREF0B2	H24	K26	H25			HIGH
IO	DIFFIO_TX36n		B2	VREF0B2	H23	L26	H26			HIGH
IO	DIFFIO_RX35p		B2	VREF0B2	D27	H29	G31			HIGH
IO	DIFFIO_RX35n		B2	VREF0B2	D28	J29	G32			HIGH
IO	DIFFIO_TX35p		B2	VREF0B2	H22	J26	J25			HIGH
IO	DIFFIO_TX35n		B2	VREF0B2	H21	H26	J26			HIGH
IO	DIFFIO_RX34p		B2	VREF0B2	E27	D30	H31			HIGH
IO	DIFFIO_RX34n		B2	VREF0B2	E28	E30	H32			HIGH
IO	DIFFIO_TX34p		B2	VREF0B2	J24	G26	K28			HIGH
IO	DIFFIO_TX34n		B2	VREF0B2	J23	F26	K27			HIGH
IO	DIFFIO_RX33p		B2	VREF1B2	F25	F30	J29			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 3 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_RX33n		B2	VREF1B2	F26	G30	J30			HIGH
IO	DIFFIO_TX33p		B2	VREF1B2	K23	F27	K26			HIGH
IO	DIFFIO_TX33n		B2	VREF1B2	K24	G27	K25			HIGH
IO	DIFFIO_RX32p		B2	VREF1B2	F27	H30	K30			HIGH
IO	DIFFIO_RX32n		B2	VREF1B2	F28	J30	K29			HIGH
IO	DIFFIO_TX32p		B2	VREF1B2	J21	H27	L27			HIGH
IO	DIFFIO_TX32n		B2	VREF1B2	J22	J27	L26			HIGH
IO	DIFFIO_RX31p		B2	VREF1B2	G26	F31	J32			HIGH
IO	DIFFIO_RX31n		B2	VREF1B2	G25	G31	J31			HIGH
IO	DIFFIO_TX31p		B2	VREF1B2	K21	K27	M26			HIGH
IO	DIFFIO_TX31n		B2	VREF1B2	K22	L27	M27			HIGH
IO	DIFFIO_RX30p		B2	VREF1B2	G27	H31	K31			HIGH
IO	DIFFIO_RX30n		B2	VREF1B2	G28	J31	L32			HIGH
IO	DIFFIO_TX30p		B2	VREF1B2	L22	L24	M24			HIGH
IO	DIFFIO_TX30n		B2	VREF1B2	L21	M24	M25			HIGH
VREF1B2			B2	VREF1B2	K20	M22	L25			
IO	DIFFIO_RX29p/RUP2		B2	VREF1B2	H26	K28	M28			HIGH
IO	DIFFIO_RX29n/RDN2		B2	VREF1B2	H25	K29	M29			HIGH
IO	DIFFIO_TX29p		B2	VREF1B2	L23	L25	N24			HIGH
IO	DIFFIO_TX29n		B2	VREF1B2	L24	M25	N23			HIGH
IO	DIFFIO_RX28p		B2	VREF1B2	H27	M28	L30			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 4 of 52)

Device					Package					
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA	DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
IO	DIFFIO_RX28n		B2	VREF1B2	H28	L28	L31			HIGH
IO	DIFFIO_TX28p		B2	VREF1B2	L20	P24	N27			HIGH
IO	DIFFIO_TX28n		B2	VREF1B2	L19	N24	N28			HIGH
IO	DIFFIO_RX27p		B2	VREF1B2	J25	M29	M31			HIGH
IO	DIFFIO_RX27n		B2	VREF1B2	J26	L29	M30			HIGH
IO	DIFFIO_TX27p		B2	VREF1B2	M22	N25	P23			HIGH
IO	DIFFIO_TX27n		B2	VREF1B2	M21	P25	P24			HIGH
IO	DIFFIO_RX26p		B2	VREF1B2	J27	P28	N29			HIGH
IO	DIFFIO_RX26n		B2	VREF1B2	J28	N28	N30			HIGH
IO	DIFFIO_TX26p		B2	VREF1B2	M24	M26	N25			HIGH
IO	DIFFIO_TX26n		B2	VREF1B2	M23	N26	N26			HIGH
IO	DIFFIO_RX25p		B2	VREF2B2	K26	N29	N31			HIGH
IO	DIFFIO_RX25n		B2	VREF2B2	K25	P29	N32			HIGH
IO	DIFFIO_TX25p		B2	VREF2B2	M20	M27	P28			HIGH
IO	DIFFIO_TX25n		B2	VREF2B2	M19	N27	P27			HIGH
IO	DIFFIO_RX24p		B2	VREF2B2	K27	L30	P29			HIGH
IO	DIFFIO_RX24n		B2	VREF2B2	K28	K30	P30			HIGH
IO	DIFFIO_TX24p		B2	VREF2B2	N26	P27	R28			HIGH
IO	DIFFIO_TX24n		B2	VREF2B2	N25	R27	R27			HIGH
IO	DIFFIO_RX23p		B2	VREF2B2	L25	N30	P31			HIGH
IO	DIFFIO_RX23n		B2	VREF2B2	L26	M30	P32			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 5 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_TX23p		B2	VREF2B2	N24	R26	P25			HIGH
IO	DIFFIO_TX23n		B2	VREF2B2	N23	P26	P26			HIGH
IO	DIFFIO_RX22p		B2	VREF2B2	L27	L31	R32			HIGH
IO	DIFFIO_RX22n		B2	VREF2B2	L28	K31	R31			HIGH
IO	DIFFIO_TX22p		B2	VREF2B2	N22	N23	R23			HIGH
IO	DIFFIO_TX22n		B2	VREF2B2	N21	P23	R24			HIGH
VREF2B2			B2	VREF2B2	P19	N22	R21			
IO	DIFFIO_RX21p		B2	VREF2B2	M25	R30	R30			HIGH
IO	DIFFIO_RX21n		B2	VREF2B2	M26	P30	R29			HIGH
IO	DIFFIO_TX21p		B2	VREF2B2	N20	T25	R25			HIGH
IO	DIFFIO_TX21n		B2	VREF2B2	N19	R25	R26			HIGH
IO	DIFFIO_RX20p		B2	VREF2B2	M27	P31	T32			HIGH
IO	DIFFIO_RX20n		B2	VREF2B2	N28	R31	T31			HIGH
IO	DIFFIO_TX20p		B2	VREF2B2			M23			LOW
IO	DIFFIO_TX20n		B2	VREF2B2			M22			LOW
CLK0n			B2	VREF2B2	N27	R28	T30			
CLK0p			B2	VREF2B2	P27	R29	T29			
IO	CLK1n		B2	VREF2B2	P26	T30	T28			
CLK1p			B2	VREF2B2	P25	T31	T27			
VCCINT										
VCCA_PLL1					P23	R24	T25			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 6 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
GND										
GNDA_PLL1					P24	T24	T26			
VCCG_PLL1					P21	R22	R22			
GNDG_PLL1					P22	R23	T22			
VCCINT										
VCCA_PLL2					R23	U24	U25			
GND										
GNDA_PLL2					R24	V24	U26			
VCCG_PLL2					R21	U23	U24			
GNDG_PLL2					R22	V23	T24			
CLK2p			B1	VREF0B1	R27	T29	U31			
CLK2n			B1	VREF0B1	T27	T28	U32			
CLK3p			B1	VREF0B1	R25	U29	U29			
IO	CLK3n		B1	VREF0B1	R26	U28	U30			
IO	DIFFIO_RX19p		B1	VREF0B1	T28	U31	U28			HIGH
IO	DIFFIO_RX19n		B1	VREF0B1	U27	V31	U27			HIGH
IO	DIFFIO_TX19p		B1	VREF0B1	T21	V25	V26			HIGH
IO	DIFFIO_TX19n		B1	VREF0B1	T22	U25	V25			HIGH
IO	DIFFIO_RX18p		B1	VREF0B1	U26	AB31	V32			HIGH
IO	DIFFIO_RX18n		B1	VREF0B1	U25	AA31	V31			HIGH
IO	DIFFIO_TX18p		B1	VREF0B1	T19	U26	V28			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 7 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_TX18n		B1	VREF0B1	T20	T26	V27			HIGH
VREF0B1			B1	VREF0B1	R19	V22	V21			
IO	DIFFIO_RX17p		B1	VREF0B1	V27	V30	V30			HIGH
IO	DIFFIO_RX17n		B1	VREF0B1	V28	U30	V29			HIGH
IO	DIFFIO_TX17p		B1	VREF0B1	T23	T27	W25			HIGH
IO	DIFFIO_TX17n		B1	VREF0B1	T24	U27	W26			HIGH
IO	DIFFIO_RX16p		B1	VREF0B1	V26	W30	W32			HIGH
IO	DIFFIO_RX16n		B1	VREF0B1	V25	Y30	W31			HIGH
IO	DIFFIO_TX16p		B1	VREF0B1	T26	V26	W27			HIGH
IO	DIFFIO_TX16n		B1	VREF0B1	T25	W26	W28			HIGH
IO	DIFFIO_RX15p		B1	VREF0B1	W28	AA30	W30			HIGH
IO	DIFFIO_RX15n		B1	VREF0B1	W27	AB30	W29			HIGH
IO	DIFFIO_TX15p		B1	VREF0B1	U19	W24	V24			HIGH
IO	DIFFIO_TX15n		B1	VREF0B1	U20	Y24	V23			HIGH
IO	DIFFIO_RX14p		B1	VREF0B1	W26	V29	Y32			HIGH
IO	DIFFIO_RX14n		B1	VREF0B1	W25	W29	Y31			HIGH
IO	DIFFIO_TX14p		B1	VREF0B1	U24	W25	Y26			HIGH
IO	DIFFIO_TX14n		B1	VREF0B1	U23	Y25	Y25			HIGH
IO	DIFFIO_RX13p		B1	VREF1B1	Y28	Y29	Y30			HIGH
IO	DIFFIO_RX13n		B1	VREF1B1	Y27	AA29	Y29			HIGH
IO	DIFFIO_TX13p		B1	VREF1B1	U21	Y26	Y28			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 8 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_TX13n		B1	VREF1B1	U22	AA26	Y27			HIGH
IO	DIFFIO_RX12p		B1	VREF1B1	Y26	V28	AA31			HIGH
IO	DIFFIO_RX12n		B1	VREF1B1	Y25	W28	AA30			HIGH
IO	DIFFIO_TX12p		B1	VREF1B1	V19	W23	W23			HIGH
IO	DIFFIO_TX12n		B1	VREF1B1	V20	Y23	W24			HIGH
IO	DIFFIO_RX11p		B1	VREF1B1	AA28	Y28	AB31			HIGH
IO	DIFFIO_RX11n		B1	VREF1B1	AA27	AA28	AB30			HIGH
IO	DIFFIO_TX11p		B1	VREF1B1	V24	V27	Y23			HIGH
IO	DIFFIO_TX11n		B1	VREF1B1	V23	W27	Y24			HIGH
IO	DIFFIO_RX10p/RUP1		B1	VREF1B1	AA25	AB29	AA28			HIGH
IO	DIFFIO_RX10n/RDN1		B1	VREF1B1	AA26	AB28	AA29			HIGH
IO	DIFFIO_TX10p		B1	VREF1B1	V22	Y27	AA25			HIGH
IO	DIFFIO_TX10n		B1	VREF1B1	V21	AA27	AA24			HIGH
VREF1B1			B1	VREF1B1	W20	W22	AA23			
IO	DIFFIO_RX9p		B1	VREF1B1	AB28	AC31	AB32			HIGH
IO	DIFFIO_RX9n		B1	VREF1B1	AB27	AD31	AC31			HIGH
IO	DIFFIO_TX9p		B1	VREF1B1	W23	AB27	AA27			HIGH
IO	DIFFIO_TX9n		B1	VREF1B1	W24	AC27	AA26			HIGH
IO	DIFFIO_RX8p		B1	VREF1B1	AB26	AE31	AD32			HIGH
IO	DIFFIO_RX8n		B1	VREF1B1	AB25	AF31	AD31			HIGH
IO	DIFFIO_TX8p		B1	VREF1B1	W21	AE27	AB27			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 9 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_TX8n		B1	VREF1B1	W22	AD27	AB26			HIGH
IO	DIFFIO_RX7p		B1	VREF1B1	AC28	AC30	AC29			HIGH
IO	DIFFIO_RX7n		B1	VREF1B1	AC27	AD30	AC30			HIGH
IO	DIFFIO_TX7p		B1	VREF1B1	Y21	AG27	AC25			HIGH
IO	DIFFIO_TX7n		B1	VREF1B1	Y22	AF27	AC26			HIGH
IO	DIFFIO_RX6p		B1	VREF1B1	AD28	AF30	AD30			HIGH
IO	DIFFIO_RX6n		B1	VREF1B1	AD27	AE30	AD29			HIGH
IO	DIFFIO_TX6p		B1	VREF1B1	Y24	AB26	AC27			HIGH
IO	DIFFIO_TX6n		B1	VREF1B1	Y23	AC26	AC28			HIGH
IO	DIFFIO_RX5p		B1	VREF2B1	AE28	AG30	AE32			HIGH
IO	DIFFIO_RX5n		B1	VREF2B1	AE27	AH30	AE31			HIGH
IO	DIFFIO_TX5p		B1	VREF2B1	AA23	AD26	AD28			HIGH
IO	DIFFIO_TX5n		B1	VREF2B1	AA24	AE26	AD27			HIGH
IO	DIFFIO_RX4p		B1	VREF2B1	AF28	AC29	AE30			HIGH
IO	DIFFIO_RX4n		B1	VREF2B1	AF27	AD29	AE29			HIGH
IO	DIFFIO_TX4p		B1	VREF2B1	AA21	AA25	AD26			HIGH
IO	DIFFIO_TX4n		B1	VREF2B1	AA22	AB25	AD25			HIGH
IO	DIFFIO_RX3p		B1	VREF2B1		AE29	AF32			HIGH
IO	DIFFIO_RX3n		B1	VREF2B1		AF29	AF31			HIGH
IO	DIFFIO_TX3p		B1	VREF2B1	AB23	AD25	AE28			HIGH
IO	DIFFIO_TX3n		B1	VREF2B1	AB24	AC25	AE27			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 10 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_RX2p		B1	VREF2B1		AH29	AF30			HIGH
IO	DIFFIO_RX2n		B1	VREF2B1		AG29	AF29			HIGH
IO	DIFFIO_TX2p		B1	VREF2B1		AA24	AE25			HIGH
IO	DIFFIO_TX2n		B1	VREF2B1		AB24	AE26			HIGH
VREF2B1			B1	VREF2B1	AE26	Y22	AB25			
IO	DIFFIO_RX1p		B1	VREF2B1		AC28	AG31			HIGH
IO	DIFFIO_RX1n		B1	VREF2B1		AD28	AG32			HIGH
IO	DIFFIO_TX1p		B1	VREF2B1		AD24	AF27			HIGH
IO	DIFFIO_TX1n		B1	VREF2B1		AC24	AF28			HIGH
IO	DIFFIO_RX0p		B1	VREF2B1		AE28	AG30			HIGH
IO	DIFFIO_RX0n		B1	VREF2B1		AF28	AG29			HIGH
IO	DIFFIO_TX0p		B1	VREF2B1		AE25	AF26			HIGH
IO	DIFFIO_TX0n		B1	VREF2B1		AF25	AF25			HIGH
FPLL8CLKn			B1	VREF2B1		AG31	AB29			
FPLL8CLKp			B1	VREF2B1		AH31	AB28			
IO			B1	VREF2B1			AA22			
IO			B1	VREF2B1			AB23			
VCCINT										
VCCA_PLL8						AB23	AJ31			
GND										
GNDA_PLL8						AA23	AJ32			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 11 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
VCCG_PLL8						AD23	AJ30			
GNDG_PLL8						AC23	AH30			
IO			B8	VREF0B8	AC24	AG28	AC24			
IO	DQ9B7		B8	VREF0B8	AG26	AK29	AH28	DQ3B15	DQ1B31	
IO			B8	VREF0B8	AC23	AJ30	AD24			
IO	DQ9B6		B8	VREF0B8	AH26	AJ29	AK30	DQ3B14	DQ1B30	
IO	DQ9B5		B8	VREF0B8	AG25	AJ28	AJ28	DQ3B13	DQ1B29	
IO	DQ9B4		B8	VREF0B8	AH25	AL28	AJ29	DQ3B12	DQ1B28	
IO			B8	VREF0B8	AB22	AA21	AB24			
IO	DQ9B3		B8	VREF0B8	AF25	AH27	AK29	DQ3B11	DQ1B27	
IO			B8	VREF0B8		AF26	AE24			
IO	DQS9B		B8	VREF0B8	AF24	AK28	AK28			
IO	DQ9B2		B8	VREF0B8	AG24	AL27	AL30	DQ3B10	DQ1B26	
IO			B8	VREF0B8	AE25	AE24	AF24			
IO	DQ9B1		B8	VREF0B8	AE24	AJ27	AL29	DQ3B9	DQ1B25	
IO			B8	VREF0B8			AC23			
IO	DQ9B0		B8	VREF0B8	AH24	AK27	AM29	DQ3B8	DQ1B24	
IO			B8	VREF0B8	AD24	AC22	AE23			
IO			B8	VREF0B8		AD22	AG24			
IO	DQ8B7		B8	VREF0B8	AG23	AH26	AH26	DQ3B7	DQ1B23	
VREF0B8			B8	VREF0B8	AD22	AB22	AH27			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 12 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DQ8B6		B8	VREF0B8	AD23	AG26	AJ27	DQ3B6	DQ1B22	
IO	DQ8B5		B8	VREF0B8	AF23	AK26	AL28	DQ3B5	DQ1B21	
IO			B8	VREF0B8	AB21	AH28	AD23			
IO	DQ8B4		B8	VREF0B8	AH23	AL26	AK27	DQ3B4	DQ1B20	
IO	DQ8B3		B8	VREF0B8	AE22	AH25	AJ26	DQ3B3	DQ1B19	
IO			B8	VREF0B8		AE22	AF23			
IO	DQS8B		B8	VREF0B8	AE23	AJ26	AL27	DQS3B		
IO	DQ8B2		B8	VREF0B8	AF22	AK25	AM27	DQ3B2	DQ1B18	
IO			B8	VREF0B8	AB20	AC21	AC22			
IO	DQ8B1		B8	VREF0B8	AH22	AJ25	AM28	DQ3B1	DQ1B17	
IO	DQ8B0		B8	VREF0B8	AG22	AL25	AK26	DQ3B0	DQ1B16	
IO			B8	VREF0B8			AG23			
IO			B8	VREF1B8	Y20	AD21	AB22			
IO	DQ7B7		B8	VREF1B8	AD21	AG24	AH24	DQ2B15	DQ1B15	
IO			B8	VREF1B8		AC20	AD22			
IO	DQ7B6		B8	VREF1B8	AE21	AH23	AJ24	DQ2B14	DQ1B14	
IO	DQ7B5		B8	VREF1B8	AG21	AK24	AJ25	DQ2B13	DQ1B13	
IO			B8	VREF1B8	AC22	AD20	AF22			
IO	DQ7B4		B8	VREF1B8	AF21	AH24	AK25	DQ2B12	DQ1B12	
IO	DQ7B3		B8	VREF1B8	AE20	AJ23	AL25	DQ2B11	DQ1B11	
IO			B8	VREF1B8			AC21			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 13 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DQS7B		B8	VREF1B8	AG20	AJ24	AL26		DQS1B	
IO	DQ7B2		B8	VREF1B8	AF20	AL24	AK24	DQ2B10	DQ1B10	
IO			B8	VREF1B8	AC20	AE20	AG22			
IO	DQ7B1		B8	VREF1B8	AH21	AK23	AM25	DQ2B9	DQ1B9	
IO			B8	VREF1B8			AB21			
IO	DQ7B0		B8	VREF1B8	AH20	AL23	AM26	DQ2B8	DQ1B8	
IO	DQ6B7		B8	VREF1B8	AE19	AG22	AJ23	DQ2B7	DQ1B7	
IO	FCLK3		B8	VREF1B8	AC21	AF23	AE21			
IO	FCLK2		B8	VREF1B8	AC19	AF22	AF21			
VREF1B8			B8	VREF1B8	AD20	AB21	AH25			
IO	DQ6B6		B8	VREF1B8	AD19	AH22	AL24	DQ2B6	DQ1B6	
IO	DQ6B5		B8	VREF1B8	AF19	AK22	AH22	DQ2B5	DQ1B5	
IO			B8	VREF1B8		AC19	AD21			
IO	DQ6B4		B8	VREF1B8	AG19	AG21	AM24	DQ2B4	DQ1B4	
IO		PGM2	B8	VREF1B8	AB19	AF24	AA20			
IO	DQ6B3		B8	VREF1B8	AH19	AH21	AK23	DQ2B3	DQ1B3	
IO			B8	VREF1B8		AA19	AA21			
IO	DQS6B		B8	VREF1B8	AF18	AJ22	AJ22	DQS2B		
IO	DQ6B2		B8	VREF1B8	AD18	AL22	AL23	DQ2B2	DQ1B2	
IO			B8	VREF1B8	AA20	AE21	AF20			
IO	DQ6B1		B8	VREF1B8	AE18	AJ21	AK22	DQ2B1	DQ1B1	

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 14 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DQ6B0		B8	VREF1B8	AG18	AK21	AL22	DQ2B0	DQ1B0	
IO	RDN8		B8	VREF1B8	Y19	AE23	AC20			
IO	RUP8		B8	VREF1B8	W19	AG25	AH19			
IO	DQ5B7		B8	VREF1B8	AF17	AG20	AM22			
IO			B8	VREF1B8		AE19	AD20			
IO	DQ5B6		B8	VREF1B8	AG17	AH20	AJ21			
IO	DQ5B5		B8	VREF1B8	AE17	AK20	AK21			
IO			B8	VREF2B8		AD19	AB20			
IO	DQ5B4		B8	VREF2B8	AD17	AL20	AL21			
IO		RDYnBSY	B8	VREF2B8	AA19	AG23	AA19			
IO	DQ5B3		B8	VREF2B8	AG16	AG19	AH20			
IO			B8	VREF2B8	AB18	AE18	AE20			
IO	DQS5B		B8	VREF2B8	AH16	AJ20	AJ20			
IO	DQ5B2		B8	VREF2B8	AD16	AH19	AK20			
IO		nCS	B8	VREF2B8	Y18	AF20	AC19			
IO	DQ5B1		B8	VREF2B8	AF16	AJ19	AL20			
IO	DQ5B0		B8	VREF2B8	AE16	AK19	AM20			
IO			B8	VREF2B8			AG21			
IO			B8	VREF2B8			AG20			
IO			B8	VREF2B8	V18		AB19			
IO			B8	VREF2B8	W18		AD19			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 15 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO		CS	B8	VREF2B8	AA18	AF21	AG19			
IO			B8	VREF2B8			AJ18			
IO			B8	VREF2B8			AH18			
IO			B8	VREF2B8			AK18			
VREF2B8			B8	VREF2B8	AH18	AB20	AH23			
IO	CLK5n		B8	VREF2B8	Y17	AH18	AJ19			
CLK5p			B8	VREF2B8	AA17	AJ18	AK19			
IO	CLK4n		B8	VREF2B8	AB17	AK18	AL19			
CLK4p			B8	VREF2B8	AC17	AL18	AM19			
PLL_ENA		PLL_ENA	B8	VREF2B8	AC18	AF19	AF19			
MSEL0		MSEL0	B8	VREF2B8	AC16	AF18	AG18			
MSEL1		MSEL1	B8	VREF2B8	W17	AG18	AE18			
MSEL2		MSEL2	B8	VREF2B8	AB15	AG17	AE19			
IO	PLL6_OUT3n		B12	VREF2B8	Y16	AL17	AM18			
IO	PLL6_OUT3p		B12	VREF2B8	W16	AK17	AL18			
IO	PLL6_OUT2n		B12	VREF2B8	AG15	AJ17	AK17			
IO	PLL6_OUT2p		B12	VREF2B8	AF15	AH17	AJ17			
IO	PLL6_FBn		B11	VREF2B8	AA15	AJ15	AM17			
IO	PLL6_FBp		B11	VREF2B8	AA14	AH15	AL17			
IO	PLL6_OUT1n		B11	VREF2B8	W15	AL15	AK16			
IO	PLL6_OUT1p		B11	VREF2B8	W14	AK15	AJ16			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 16 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	PLL6_OUT0n		B11	VREF2B8	AE15	AL16	AM16			
IO	PLL6_OUT0p		B11	VREF2B8	AD15	AK16	AL16			
VCC_PLL6_OUTB			B12		AB16	AC18	AB17			
VCC_PLL6_OUTB			B12							
VCC_PLL6_OUTA			B11		AC14	AD17	AE17			
VCC_PLL6_OUTA			B11							
VCCINT										
VCCA_PLL6					AG14	AB17	AG17			
GND										
GNDA_PLL6					AF14	AC17	AH17			
VCCG_PLL6					AA13	AD15	AD16			
GNDG_PLL6					AB14	AD16	AB16			
CLK7p			B7	VREF0B7	W13	AJ14	AM15			
IO	CLK7n		B7	VREF0B7	Y13	AH14	AL15			
CLK6p			B7	VREF0B7	AD14	AL14	AK15			
IO	CLK6n		B7	VREF0B7	AE14	AK14	AJ15			
nCE		nCE	B7	VREF0B7	AB13	AF17	AF18			
nCEO		nCEO	B7	VREF0B7	AC13	AF16	AH15			
IO			B7	VREF0B7		AA16	AA18			
IO			B7	VREF0B7		AA15	AC18			
IO		PGM0	B7	VREF0B7	W12	AE17	AD18			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 17 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
nIO_PULLUP		nIO_PULLUP	B7	VREF0B7	Y12	AE16	AF15			
VCCSEL		VCCSEL	B7	VREF0B7	AA12	AE15	AJ14			
PORSEL		PORSEL	B7	VREF0B7	AC12	AG16	AG15			
IO			B7	VREF0B7		AH16	AC15			
IO			B7	VREF0B7			AB15			
IO			B7	VREF0B7			AD15			
IO			B7	VREF0B7			AE14			
IO			B7	VREF0B7			AL14			
IO			B7	VREF0B7		AE13	AK14			
VREF0B7			B7	VREF0B7	AD11	AB14	AH12			
IO		INIT_DONE	B7	VREF0B7	W11	AF15	AE15			
IO			B7	VREF0B7	V11	AC13	AA15			
IO	DQ4B7		B7	VREF0B7	AD13	AK13	AL13			
IO	DQ4B6		B7	VREF0B7	AE13	AG13	AM13			
IO		nRS	B7	VREF0B7	AC11	AE14	AB18			
IO	DQ4B5		B7	VREF0B7	AF13	AH13	AH13			
IO			B7	VREF0B7	Y11	AE12	AB14			
IO	DQ4B4		B7	VREF0B7	AD12	AJ13	AJ13			
IO	DQ4B3		B7	VREF0B7	AG13	AK12	AK13			
IO		RUnLU	B7	VREF0B7	W10	AJ16	AF14			
IO	DQS4B		B7	VREF0B7	AH13	AJ12	AJ12			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 18 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO			B7	VREF0B7	AB12	AD13	AD14			
IO	DQ4B2		B7	VREF1B7	AE12	AL12	AK12			
IO	DQ4B1		B7	VREF1B7	AF12	AG12	AL12			
IO		PGM1	B7	VREF1B7	AA11	AG15	AG14			
IO	DQ4B0		B7	VREF1B7	AG12	AH12	AM11			
IO	RDN7		B7	VREF1B7	AC10	AG14	AC14			
IO	RUP7		B7	VREF1B7	AB11	AF13	AF13			
IO	DQ3B7		B7	VREF1B7	AG11	AL10	AL10	DQ1B15	DQ0B31	
IO			B7	VREF1B7		AE11	AA14			
IO	DQ3B6		B7	VREF1B7	AH11	AJ11	AK11	DQ1B14	DQ0B30	
IO	DQ3B5		B7	VREF1B7	AE11	AK11	AL11	DQ1B13	DQ0B29	
IO	DEV_CLRn		B7	VREF1B7	AC9	AF14	AH14			
IO	DQ3B4		B7	VREF1B7	AF11	AG11	AK10	DQ1B12	DQ0B28	
IO	DQ3B3		B7	VREF1B7	AE10	AH11	AM9	DQ1B11	DQ0B27	
IO			B7	VREF1B7		AD11	AB13			
IO	DQS3B		B7	VREF1B7	AG10	AJ10	AJ11	DQS1B		
IO			B7	VREF1B7	Y10	AD12	AD13			
IO	DQ3B2		B7	VREF1B7	AH10	AG10	AL9	DQ1B10	DQ0B26	
IO	DQ3B1		B7	VREF1B7	AF10	AH10	AJ10	DQ1B9	DQ0B25	
VREF1B7			B7	VREF1B7	AD9	AB13	AH10			
IO	DQ3B0		B7	VREF1B7	AD10	AK10	AH11	DQ1B8	DQ0B24	

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 19 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO			B7	VREF1B7		AA13	AC13			
IO			B7	VREF1B7	AA10	AF10	AG13			
IO	DQ2B7		B7	VREF1B7	AG9	AL8	AL8	DQ1B7	DQ0B23	
IO	FCLK5		B7	VREF1B7	AC8	AF12	AM14			
IO	FCLK4		B7	VREF1B7	AB10	AF11	AF12			
IO	DQ2B6		B7	VREF1B7	AF9	AK9	AJ9	DQ1B6	DQ0B22	
IO	DQ2B5		B7	VREF1B7	AE9	AL9	AK9	DQ1B5	DQ0B21	
IO			B7	VREF1B7	AB9	AC12	AE13			
IO	DQ2B4		B7	VREF1B7	AH8	AH8	AM8	DQ1B4	DQ0B20	
IO	DQ2B3		B7	VREF1B7	AH9	AK8	AH9	DQ1B3	DQ0B19	
IO			B7	VREF1B7		AG9	AG12			
IO	DQS2B		B7	VREF2B7	AE8	AJ8	AK8		DQS0B	
IO	DQ2B2		B7	VREF2B7	AD8	AG8	AM7	DQ1B2	DQ0B18	
IO			B7	VREF2B7	AA9	AC11	AD12			
IO	DQ2B1		B7	VREF2B7	AF8	AH9	AJ8	DQ1B1	DQ0B17	
IO	DQ2B0		B7	VREF2B7	AG8	AJ9	AL7	DQ1B0	DQ0B16	
IO			B7	VREF2B7		AE10	AE12			
IO			B7	VREF2B7	AB8	AE9	AC12			
IO	DQ1B7		B7	VREF2B7	AF6	AK7	AL6	DQ0B15	DQ0B15	
IO	DQ1B6		B7	VREF2B7	AG7	AL7	AM6	DQ0B14	DQ0B14	
IO			B7	VREF2B7	AC7	AD10	AG11			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 20 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DQ1B5		B7	VREF2B7	AH7	AH6	AJ7	DQ0B13	DQ0B13	
IO	DQ1B4		B7	VREF2B7	AF7	AK6	AM5	DQ0B12	DQ0B12	
IO			B7	VREF2B7		AC10	AA12			
IO	DQ1B3		B7	VREF2B7	AD6	AL6	AK7	DQ0B11	DQ0B11	
IO	DQS1B		B7	VREF2B7	AE7	AJ6	AH7	DQS0B		
IO			B7	VREF2B7	AD5	AG7	AE11			
IO	DQ1B2		B7	VREF2B7	AH6	AH7	AL5	DQ0B10	DQ0B10	
IO	DQ1B1		B7	VREF2B7	AG6	AJ7	AK6	DQ0B9	DQ0B9	
VREF2B7			B7	VREF2B7	AD7	AB12	AH8			
IO	DQ1B0		B7	VREF2B7	AE6	AG6	AJ6	DQ0B8	DQ0B8	
IO			B7	VREF2B7	Y9	AA11	AB11			
IO			B7	VREF2B7		AF8	AF10			
IO	DQ0B7		B7	VREF2B7	AF5	AL4	AL3	DQ0B7	DQ0B7	
IO			B7	VREF2B7	AE4	AF9	AG10			
IO	DQ0B6		B7	VREF2B7	AH5	AL5	AL4	DQ0B6	DQ0B6	
IO			B7	VREF2B7	AC6	AF6	AC9			
IO	DQ0B5		B7	VREF2B7	AF4	AJ4	AM4	DQ0B5	DQ0B5	
IO	DQ0B4		B7	VREF2B7	AG4	AK3	AJ4	DQ0B4	DQ0B4	
IO			B7	VREF2B7		AH4	AG9			
IO	DQ0B3		B7	VREF2B7	AG5	AK5	AJ5	DQ0B3	DQ0B3	
IO	DQS0B		B7	VREF2B7	AH3	AK4	AK5			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 21 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO			B7	VREF2B7	AC5	AG4	AD9			
IO	DQ0B2		B7	VREF2B7	AG3	AH5	AH5	DQ0B2	DQ0B2	
IO	DQ0B1		B7	VREF2B7	AE5	AJ5	AK3	DQ0B1	DQ0B1	
IO			B7	VREF2B7	AB7	AJ2	AE9			
IO	DQ0B0		B7	VREF2B7	AH4	AJ3	AK4	DQ0B0	DQ0B0	
IO			B7	VREF2B7		AE8	AF9			
GNDG_PLL9						AC9	AH3			
VCCG_PLL9						AD9	AJ3			
GNDA_PLL9						AA9	AJ1			
GND										
VCCA_PLL9						AB9	AJ2			
VCCINT										
IO			B6	VREF0B6			AB9			
IO			B6	VREF0B6			AC10			
FPLL9CLKp			B6	VREF0B6		AH1	AB5			
FPLL9CLKn			B6	VREF0B6		AG1	AB4			
IO	DIFFIO_TX81n		B6	VREF0B6		AC8	AF8			HIGH
IO	DIFFIO_TX81p		B6	VREF0B6		AD8	AF7			HIGH
IO	DIFFIO_RX81n		B6	VREF0B6		AF4	AG4			HIGH
IO	DIFFIO_RX81p		B6	VREF0B6		AE4	AG3			HIGH
IO	DIFFIO_TX80n		B6	VREF0B6		AF7	AF5			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 22 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_TX80p		B6	VREF0B6		AE7	AF6			HIGH
IO	DIFFIO_RX80n		B6	VREF0B6		AD4	AG1			HIGH
IO	DIFFIO_RX80p		B6	VREF0B6		AC4	AG2			HIGH
VREF0B6			B6	VREF0B6	AE3	AA10	AG6			
IO	DIFFIO_TX79n		B6	VREF0B6		AB8	AE7			HIGH
IO	DIFFIO_TX79p		B6	VREF0B6		AA8	AE8			HIGH
IO	DIFFIO_RX79n		B6	VREF0B6		AG3	AF4			HIGH
IO	DIFFIO_RX79p		B6	VREF0B6		AH3	AF3			HIGH
IO	DIFFIO_TX78n		B6	VREF0B6	AB5	AC7	AD6			HIGH
IO	DIFFIO_TX78p		B6	VREF0B6	AB6	AD7	AD5			HIGH
IO	DIFFIO_RX78n		B6	VREF0B6		AF3	AF2			HIGH
IO	DIFFIO_RX78p		B6	VREF0B6		AE3	AF1			HIGH
IO	DIFFIO_TX77n		B6	VREF0B6	AA7	AB7	AE6			HIGH
IO	DIFFIO_TX77p		B6	VREF0B6	AA8	AA7	AE5			HIGH
IO	DIFFIO_RX77n		B6	VREF0B6	AF2	AD3	AE4			HIGH
IO	DIFFIO_RX77p		B6	VREF0B6	AF1	AC3	AE3			HIGH
IO	DIFFIO_TX76n		B6	VREF0B6	AA5	AE6	AD8			HIGH
IO	DIFFIO_TX76p		B6	VREF0B6	AA6	AD6	AD7			HIGH
IO	DIFFIO_RX76n		B6	VREF0B6	AE2	AH2	AE2			HIGH
IO	DIFFIO_RX76p		B6	VREF0B6	AE1	AG2	AE1			HIGH
IO	DIFFIO_TX75n		B6	VREF1B6	Y6	AC6	AC5			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 23 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_TX75p		B6	VREF1B6	Y5	AB6	AC6			HIGH
IO	DIFFIO_RX75n		B6	VREF1B6	AD2	AE2	AC3			HIGH
IO	DIFFIO_RX75p		B6	VREF1B6	AD1	AF2	AC4			HIGH
IO	DIFFIO_TX74n		B6	VREF1B6	Y7	AF5	AC7			HIGH
IO	DIFFIO_TX74p		B6	VREF1B6	Y8	AG5	AC8			HIGH
IO	DIFFIO_RX74n		B6	VREF1B6	AC2	AD2	AD3			HIGH
IO	DIFFIO_RX74p		B6	VREF1B6	AC1	AC2	AD4			HIGH
IO	DIFFIO_TX73n		B6	VREF1B6	W7	AD5	AB7			HIGH
IO	DIFFIO_TX73p		B6	VREF1B6	W8	AE5	AB6			HIGH
IO	DIFFIO_RX73n		B6	VREF1B6	AB4	AF1	AD2			HIGH
IO	DIFFIO_RX73p		B6	VREF1B6	AB3	AE1	AD1			HIGH
IO	DIFFIO_TX72n		B6	VREF1B6	W5	AC5	AA6			HIGH
IO	DIFFIO_TX72p		B6	VREF1B6	W6	AB5	AA7			HIGH
IO	DIFFIO_RX72n		B6	VREF1B6	AB2	AD1	AC2			HIGH
IO	DIFFIO_RX72p		B6	VREF1B6	AB1	AC1	AB1			HIGH
VREF1B6			B6	VREF1B6	W9	Y10	AB8			
IO	DIFFIO_TX71n		B6	VREF1B6	V8	AA6	AA9			HIGH
IO	DIFFIO_TX71p		B6	VREF1B6	V7	Y6	AA8			HIGH
IO	DIFFIO_RX71n/RDN6		B6	VREF1B6	AA3	AB4	AA4			HIGH
IO	DIFFIO_RX71p/RUP6		B6	VREF1B6	AA4	AB3	AA5			HIGH
IO	DIFFIO_TX70n		B6	VREF1B6	V6	Y9	Y5			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 24 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_TX70p		B6	VREF1B6	V5	W9	Y6			HIGH
IO	DIFFIO_RX70n		B6	VREF1B6	AA2	Y4	AB3			HIGH
IO	DIFFIO_RX70p		B6	VREF1B6	AA1	AA4	AB2			HIGH
IO	DIFFIO_TX69n		B6	VREF1B6	V9	Y8	Y7			HIGH
IO	DIFFIO_TX69p		B6	VREF1B6	V10	W8	Y8			HIGH
IO	DIFFIO_RX69n		B6	VREF1B6	Y4	W4	AA3			HIGH
IO	DIFFIO_RX69p		B6	VREF1B6	Y3	V4	AA2			HIGH
IO	DIFFIO_TX68n		B6	VREF1B6	U7	AA5	W5			HIGH
IO	DIFFIO_TX68p		B6	VREF1B6	U8	Y5	W6			HIGH
IO	DIFFIO_RX68n		B6	VREF1B6	Y2	AA3	Y4			HIGH
IO	DIFFIO_RX68p		B6	VREF1B6	Y1	Y3	Y3			HIGH
IO	DIFFIO_TX67n		B6	VREF2B6	U6	Y7	Y10			HIGH
IO	DIFFIO_TX67p		B6	VREF2B6	U5	W7	Y9			HIGH
IO	DIFFIO_RX67n		B6	VREF2B6	W4	W3	Y2			HIGH
IO	DIFFIO_RX67p		B6	VREF2B6	W3	V3	Y1			HIGH
IO	DIFFIO_TX66n		B6	VREF2B6	U9	U7	W10			HIGH
IO	DIFFIO_TX66p		B6	VREF2B6	U10	V7	W9			HIGH
IO	DIFFIO_RX66n		B6	VREF2B6	W2	AB2	W4			HIGH
IO	DIFFIO_RX66p		B6	VREF2B6	W1	AA2	W3			HIGH
IO	DIFFIO_TX65n		B6	VREF2B6	T6	W6	V9			HIGH
IO	DIFFIO_TX65p		B6	VREF2B6	T5	V6	V10			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 25 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_RX65n		B6	VREF2B6	V4	Y2	W2			HIGH
IO	DIFFIO_RX65p		B6	VREF2B6	V3	W2	W1			HIGH
IO	DIFFIO_TX64n		B6	VREF2B6	T10	U6	V5			HIGH
IO	DIFFIO_TX64p		B6	VREF2B6	T9	T6	V6			HIGH
IO	DIFFIO_RX64n		B6	VREF2B6	V1	AA1	V4			HIGH
IO	DIFFIO_RX64p		B6	VREF2B6	V2	AB1	V3			HIGH
VREF2B6			B6	VREF2B6	R10	W10	AA10			
IO	DIFFIO_TX63n		B6	VREF2B6	T7	W5	V8			HIGH
IO	DIFFIO_TX63p		B6	VREF2B6	T8	V5	V7			HIGH
IO	DIFFIO_RX63n		B6	VREF2B6	U4	V2	V2			HIGH
IO	DIFFIO_RX63p		B6	VREF2B6	U3	U2	V1			HIGH
IO	DIFFIO_TX62n		B6	VREF2B6	T4	T5	W8			HIGH
IO	DIFFIO_TX62p		B6	VREF2B6	T3	U5	W7			HIGH
IO	DIFFIO_RX62n		B6	VREF2B6	U2	V1	U5			HIGH
IO	DIFFIO_RX62p		B6	VREF2B6	T1	U1	U6			HIGH
IO	CLK8n		B6	VREF2B6	R3	U4	U3			
CLK8p			B6	VREF2B6	R4	U3	U4			
CLK9n			B6	VREF2B6	T2	T3	U1			
CLK9p			B6	VREF2B6	R2	T4	U2			
GNDG_PLL3					R7	V9	U11			
VCCG_PLL3					R8	U9	V11			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 26 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
GNDA_PLL3					R5	V8	U7			
GND										
VCCA_PLL3					R6	U8	U8			
VCCINT										
GNDG_PLL4					P7	R9	U9			
VCCG_PLL4					P8	R10	T9			
GNDA_PLL4					P5	R8	T7			
GND										
VCCA_PLL4					P6	T8	T8			
VCCINT										
CLK10p			B5	VREF0B5	P4	T1	T6			
IO	CLK10n		B5	VREF0B5	P3	T2	T5			
CLK11p			B5	VREF0B5	P2	R3	T4			
CLK11n			B5	VREF0B5	N2	R4	T3			
IO	DIFFIO_TX61n		B5	VREF0B5			T11			LOW
IO	DIFFIO_TX61p		B5	VREF0B5			R11			LOW
IO	DIFFIO_RX61n		B5	VREF0B5	M2	R1	T2			HIGH
IO	DIFFIO_RX61p		B5	VREF0B5	N1	P1	T1			HIGH
IO	DIFFIO_TX60n		B5	VREF0B5	N10	R7	R7			HIGH
IO	DIFFIO_TX60p		B5	VREF0B5	N9	T7	R8			HIGH
IO	DIFFIO_RX60n		B5	VREF0B5	M3	P2	R1			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 27 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_RX60p		B5	VREF0B5	M4	R2	R2			HIGH
VREF0B5			B5	VREF0B5	P10	P10	R12			
IO	DIFFIO_TX59n		B5	VREF0B5	N5	P8	P7			HIGH
IO	DIFFIO_TX59p		B5	VREF0B5	N6	N8	P8			HIGH
IO	DIFFIO_RX59n		B5	VREF0B5	L1	K1	R3			HIGH
IO	DIFFIO_RX59p		B5	VREF0B5	L2	L1	R4			HIGH
IO	DIFFIO_TX58n		B5	VREF0B5	N7	R6	R5			HIGH
IO	DIFFIO_TX58p		B5	VREF0B5	N8	P6	R6			HIGH
IO	DIFFIO_RX58n		B5	VREF0B5	L3	N2	P1			HIGH
IO	DIFFIO_RX58p		B5	VREF0B5	L4	M2	P2			HIGH
IO	DIFFIO_TX57n		B5	VREF0B5	N4	P9	R10			HIGH
IO	DIFFIO_TX57p		B5	VREF0B5	N3	N9	R9			HIGH
IO	DIFFIO_RX57n		B5	VREF0B5	K1	L2	P3			HIGH
IO	DIFFIO_RX57p		B5	VREF0B5	K2	K2	P4			HIGH
IO	DIFFIO_TX56n		B5	VREF0B5	M10	P7	P6			HIGH
IO	DIFFIO_TX56p		B5	VREF0B5	M9	N7	P5			HIGH
IO	DIFFIO_RX56n		B5	VREF0B5	K4	P3	N1			HIGH
IO	DIFFIO_RX56p		B5	VREF0B5	K3	N3	N2			HIGH
IO	DIFFIO_TX55n		B5	VREF1B5	M6	N6	N7			HIGH
IO	DIFFIO_TX55p		B5	VREF1B5	M5	M6	N8			HIGH
IO	DIFFIO_RX55n		B5	VREF1B5	J1	L3	N3			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 28 of 52)

Device					Package					
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA	DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
IO	DIFFIO_RX55p		B5	VREF1B5	J2	M3	N4			HIGH
IO	DIFFIO_TX54n		B5	VREF1B5	M8	R5	P9			HIGH
IO	DIFFIO_TX54p		B5	VREF1B5	M7	P5	P10			HIGH
IO	DIFFIO_RX54n		B5	VREF1B5	J3	P4	M2			HIGH
IO	DIFFIO_RX54p		B5	VREF1B5	J4	N4	M3			HIGH
IO	DIFFIO_TX53n		B5	VREF1B5	L10	M5	N5			HIGH
IO	DIFFIO_TX53p		B5	VREF1B5	L9	N5	N6			HIGH
IO	DIFFIO_RX53n		B5	VREF1B5	H1	M4	L2			HIGH
IO	DIFFIO_RX53p		B5	VREF1B5	H2	L4	L3			HIGH
IO	DIFFIO_TX52n		B5	VREF1B5	L5	M8	N10			HIGH
IO	DIFFIO_TX52p		B5	VREF1B5	L6	L8	N9			HIGH
IO	DIFFIO_RX52n/RDN5		B5	VREF1B5	H3	K3	M4			HIGH
IO	DIFFIO_RX52p/RUP5		B5	VREF1B5	H4	K4	M5			HIGH
VREF1B5			B5	VREF1B5	K9	N10	L8			
IO	DIFFIO_TX51n		B5	VREF1B5	L8	M7	M8			HIGH
IO	DIFFIO_TX51p		B5	VREF1B5	L7	L7	M9			HIGH
IO	DIFFIO_RX51n		B5	VREF1B5	G1	J1	L1			HIGH
IO	DIFFIO_RX51p		B5	VREF1B5	G2	H1	K2			HIGH
IO	DIFFIO_TX50n		B5	VREF1B5	K7	L5	M6			HIGH
IO	DIFFIO_TX50p		B5	VREF1B5	K8	K5	M7			HIGH
IO	DIFFIO_RX50n		B5	VREF1B5	G4	G1	J2			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 29 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_RX50p		B5	VREF1B5	G3	F1	J1			HIGH
IO	DIFFIO_TX49n		B5	VREF1B5	J7	H5	L6			HIGH
IO	DIFFIO_TX49p		B5	VREF1B5	J8	J5	L7			HIGH
IO	DIFFIO_RX49n		B5	VREF1B5	F1	H2	K4			HIGH
IO	DIFFIO_RX49p		B5	VREF1B5	F2	J2	K3			HIGH
IO	DIFFIO_TX48n		B5	VREF1B5	K5	F5	K5			HIGH
IO	DIFFIO_TX48p		B5	VREF1B5	K6	G5	K6			HIGH
IO	DIFFIO_RX48n		B5	VREF1B5	F3	G2	J3			HIGH
IO	DIFFIO_RX48p		B5	VREF1B5	F4	F2	J4			HIGH
IO	DIFFIO_TX47n		B5	VREF2B5	J6	L6	K8			HIGH
IO	DIFFIO_TX47p		B5	VREF2B5	J5	K6	K7			HIGH
IO	DIFFIO_RX47n		B5	VREF2B5	E1	J3	H1			HIGH
IO	DIFFIO_RX47p		B5	VREF2B5	E2	H3	H2			HIGH
IO	DIFFIO_TX46n		B5	VREF2B5	H8	J6	J5			HIGH
IO	DIFFIO_TX46p		B5	VREF2B5	H7	H6	J6			HIGH
IO	DIFFIO_RX46n		B5	VREF2B5	D1	G3	G1			HIGH
IO	DIFFIO_RX46p		B5	VREF2B5	D2	F3	G2			HIGH
IO	DIFFIO_TX45n		B5	VREF2B5	H6	G6	J7			HIGH
IO	DIFFIO_TX45p		B5	VREF2B5	H5	F6	J8			HIGH
IO	DIFFIO_RX45n		B5	VREF2B5	C1	J4	H3			HIGH
IO	DIFFIO_RX45p		B5	VREF2B5	C2	H4	H4			HIGH

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 30 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DIFFIO_TX44n		B5	VREF2B5	G5	K8	H5			HIGH
IO	DIFFIO_TX44p		B5	VREF2B5	G6	J8	H6			HIGH
IO	DIFFIO_RX44n		B5	VREF2B5		G4	F1			HIGH
IO	DIFFIO_RX44p		B5	VREF2B5		F4	F2			HIGH
VREF2B5			B5	VREF2B5	E5	M10	F6			
IO	DIFFIO_TX43n		B5	VREF2B5	F6	K7	H8			HIGH
IO	DIFFIO_TX43p		B5	VREF2B5	F5	J7	H7			HIGH
IO	DIFFIO_RX43n		B5	VREF2B5		E2	G3			HIGH
IO	DIFFIO_RX43p		B5	VREF2B5		D2	G4			HIGH
IO	DIFFIO_TX42n		B5	VREF2B5		H7	G6			HIGH
IO	DIFFIO_TX42p		B5	VREF2B5		G7	G5			HIGH
IO	DIFFIO_RX42n		B5	VREF2B5		E3	F3			HIGH
IO	DIFFIO_RX42p		B5	VREF2B5		D3	F4			HIGH
IO	DIFFIO_TX41n		B5	VREF2B5		G8	G7			HIGH
IO	DIFFIO_TX41p		B5	VREF2B5		H8	G8			HIGH
IO	DIFFIO_RX41n		B5	VREF2B5			E2			LOW
IO	DIFFIO_RX41p		B5	VREF2B5			E1			LOW
IO			B5	VREF2B5						
IO			B5	VREF2B5						
FPLL10CLKn			B5	VREF2B5		D1	L5			
FPLL10CLKp			B5	VREF2B5		E1	L4			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 31 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
GNDG_PLL10						K9	E3			
VCCG_PLL10						J9	D3			
GNDA_PLL10						M9	D1			
GND										
VCCA_PLL10						L9	D2			
VCCINT										
IO			B4	VREF0B4		F7	F7			
IO	DQ0T0		B4	VREF0B4	A4	C4	D5	DQ0T0	DQ0T0	
IO			B4	VREF0B4	G7	E4	K9			
IO	DQ0T1		B4	VREF0B4	A3	C5	C3	DQ0T1	DQ0T1	
IO	DQ0T2		B4	VREF0B4	B3	D5	E5	DQ0T2	DQ0T2	
IO	DQS0T		B4	VREF0B4	D5	B4	C5			
IO			B4	VREF0B4	F7	H9	H9			
IO	DQ0T3		B4	VREF0B4	B5	B5	C4	DQ0T3	DQ0T3	
IO			B4	VREF0B4		E5	J9			
IO	DQ0T4		B4	VREF0B4	B4	B3	D4	DQ0T4	DQ0T4	
IO	DQ0T5		B4	VREF0B4	C4	C3	A4	DQ0T5	DQ0T5	
IO			B4	VREF0B4	G8	C2	L9			
IO	DQ0T6		B4	VREF0B4	A5	A5	B4	DQ0T6	DQ0T6	
IO			B4	VREF0B4	F8	F8	G9			
IO	DQ0T7		B4	VREF0B4	C5	A4	B3	DQ0T7	DQ0T7	

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 32 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO			B4	VREF0B4		E7	F8			
IO			B4	VREF0B4	J9	L11	M10			
IO	DQ1T0		B4	VREF0B4	E6	E6	D6	DQ0T8	DQ0T8	
VREF0B4			B4	VREF0B4	E7	K10	E6			
IO	DQ1T1		B4	VREF0B4	A6	C7	C6	DQ0T9	DQ0T9	
IO	DQ1T2		B4	VREF0B4	B7	D7	B5	DQ0T10	DQ0T10	
IO			B4	VREF0B4		J10	J11			
IO	DQS1T		B4	VREF0B4	B6	C6	E7	DQS0T		
IO			B4	VREF0B4	H9	D4	K11			
IO	DQ1T3		B4	VREF0B4	D6	A6	C7	DQ0T11	DQ0T11	
IO	DQ1T4		B4	VREF0B4	A7	B6	A5	DQ0T12	DQ0T12	
IO			B4	VREF0B4		J11	G10			
IO	DQ1T5		B4	VREF0B4	D7	D6	D7	DQ0T13	DQ0T13	
IO			B4	VREF0B4	G9	G9	F9			
IO	DQ1T6		B4	VREF0B4	C6	A7	A6	DQ0T14	DQ0T14	
IO	DQ1T7		B4	VREF0B4	C7	B7	B6	DQ0T15	DQ0T15	
IO			B4	VREF0B4	F9	G10	F10			
IO			B4	VREF0B4		F9	H11			
IO	DQ2T0		B4	VREF0B4	D8	B8	B7	DQ1T0	DQ0T16	
IO	DQ2T1		B4	VREF0B4	C8	D9	D8	DQ1T1	DQ0T17	
IO			B4	VREF0B4	H10	H10	L11			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 33 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DQ2T2		B4	VREF0B4	E8	E8	B8	DQ1T2	DQ0T18	
IO	DQS2T		B4	VREF1B4	C9	C8	A7		DQS0T	
IO			B4	VREF1B4		H11	F12			
IO	DQ2T3		B4	VREF1B4	D9	C9	E9	DQ1T3	DQ0T19	
IO	DQ2T4		B4	VREF1B4	B9	D8	A8	DQ1T4	DQ0T20	
IO	DQ2T5		B4	VREF1B4	B8	A9	C9	DQ1T5	DQ0T21	
IO	DQ2T6		B4	VREF1B4	A8	B9	C8	DQ1T6	DQ0T22	
IO	FCLK6		B4	VREF1B4	G10	F10	G12			
IO	FCLK7		B4	VREF1B4	F10	F11	A14			
IO	DQ2T7		B4	VREF1B4	A9	A8	D9	DQ1T7	DQ0T23	
IO			B4	VREF1B4		J12	J12			
IO			B4	VREF1B4	J10	L12	K12			
IO	DQ3T0		B4	VREF1B4	E10	B10	E11	DQ1T8	DQ0T24	
VREF1B4			B4	VREF1B4	E9	K11	E8			
IO	DQ3T1		B4	VREF1B4	A10	D10	B9	DQ1T9	DQ0T25	
IO			B4	VREF1B4	F11	H12	H13			
IO	DQ3T2		B4	VREF1B4	C10	E10	D10	DQ1T10	DQ0T26	
IO			B4	VREF1B4	K10	E9	H12			
IO	DQS3T		B4	VREF1B4	D10	C10	D11	DQS1T		
IO	DQ3T3		B4	VREF1B4	B10	D11	C10	DQ1T11	DQ0T27	
IO			B4	VREF1B4		G11	F13			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 34 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DQ3T4		B4	VREF1B4	A11	E11	A9	DQ1T12	DQ0T28	
IO	DQ3T5		B4	VREF1B4	C11	B11	B11	DQ1T13	DQ0T29	
IO	DEV_OE		B4	VREF1B4	J11	F12	L13			
IO	DQ3T6		B4	VREF1B4	D11	C11	C11	DQ1T14	DQ0T30	
IO	DQ3T7		B4	VREF1B4	B11	A10	B10	DQ1T15	DQ0T31	
IO	RUP4		B4	VREF1B4	H11	F13	G13			
IO	RDN4		B4	VREF1B4	G11	E14	J13			
IO	DQ4T0		B4	VREF1B4	B12	D12	A11			
IO		nWS	B4	VREF1B4	K11	F14	D14			
IO	DQ4T1		B4	VREF1B4	C12	E12	B12			
IO	DQ4T2		B4	VREF1B4	D12	A12	C12			
IO			B4	VREF2B4	G12	G12	H14			
IO	DQS4T		B4	VREF2B4	A13	C12	D12			
IO		DATA0	B4	VREF2B4	H12	E15	E14			
IO	DQ4T3		B4	VREF2B4	B13	B12	C13			
IO	DQ4T4		B4	VREF2B4	E12	C13	D13			
IO			B4	VREF2B4	L11	J13	K13			
IO	DQ4T5		B4	VREF2B4	C13	D13	E13			
IO		DATA1	B4	VREF2B4	F12	C16	F14			
IO	DQ4T6		B4	VREF2B4	D13	E13	A13			
IO	DQ4T7		B4	VREF2B4	E13	B13	B13			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 35 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO			B4	VREF2B4	M11	L14	L12			
IO		DATA2	B4	VREF2B4	J12	F15	F15			
VREF2B4			B4	VREF2B4	E11	K12	E10			
IO			B4	VREF2B4		G13	C14			
IO			B4	VREF2B4			B14			
IO			B4	VREF2B4			K14			
IO			B4	VREF2B4			J14			
IO			B4	VREF2B4			L14			
IO			B4	VREF2B4		H13	K15			
TMS		TMS	B4	VREF2B4	F13	D16	E15			
TRST		TRST	B4	VREF2B4	L12	G15	G15			
TCK		TCK	B4	VREF2B4	K12	F16	G14			
IO		DATA3	B4	VREF2B4	M12	G17	C16			
IO			B4	VREF2B4		G14	J15			
IO			B4	VREF2B4		L16	L15			
TDI		TDI	B4	VREF2B4	G13	E16	D16			
TDO		TDO	B4	VREF2B4	H13	G16	F16			
IO	CLK12n		B4	VREF2B4	J13	B14	A15			
CLK12p			B4	VREF2B4	K13	A14	B15			
IO	CLK13n		B4	VREF2B4	L13	D14	C15			
CLK13p			B4	VREF2B4	M13	C14	D15			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 36 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
TEMPDIODEp					B14	E17	E18			
TEMPDIODEn					C14	F17	F18			
VCCINT										
VCCA_PLL5					F14	J17	G17			
GND										
GNDA_PLL5					G14	H16	F17			
VCCG_PLL5					D14	K15	J16			
GNDG_PLL5					E14	K17	L16			
VCC_PLL5_OUTA			B9		F15	L18	H17			
VCC_PLL5_OUTA			B9							
VCC_PLL5_OUTB			B10		G16	J18	L17			
VCC_PLL5_OUTB			B10							
IO	PLL5_OUT0p		B9	VREF0B3	E15	B16	B16			
IO	PLL5_OUT0n		B9	VREF0B3	D15	A16	A16			
IO	PLL5_OUT1p		B9	VREF0B3	K14	B15	B17			
IO	PLL5_OUT1n		B9	VREF0B3	K15	A15	A17			
IO	PLL5_FBp		B9	VREF0B3	H14	D15	D17			
IO	PLL5_FBn		B9	VREF0B3	H15	C15	C17			
IO	PLL5_OUT2p		B10	VREF0B3	C15	D17	B18			
IO	PLL5_OUT2n		B10	VREF0B3	B15	C17	A18			
IO	PLL5_OUT3p		B10	VREF0B3	K16	B17	D18			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 37 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	PLL5_OUT3n		B10	VREF0B3	J16	A17	C18			
nSTATUS		nSTATUS	B3	VREF0B3	M16	E18	G16			
nCONFIG		nCONFIG	B3	VREF0B3	L16	F19	J18			
DCLK		DCLK	B3	VREF0B3	F16	F18	E19			
CONF_DONE		CONF_DONE	B3	VREF0B3	G17	G18	G18			
CLK14p			B3	VREF0B3	K17	A18	A19			
IO	CLK14n		B3	VREF0B3	J17	B18	B19			
CLK15p			B3	VREF0B3	M17	C18	C19			
IO	CLK15n		B3	VREF0B3	L17	D18	D19			
VREF0B3			B3	VREF0B3	E18	K18	E21			
IO			B3	VREF0B3			K18			
IO			B3	VREF0B3			F19			
IO		DATA4	B3	VREF0B3	H17	G19	G19			
IO			B3	VREF0B3	L18	H20	L18			
IO			B3	VREF0B3	M18	J19	L21			
IO			B3	VREF0B3			L20			
IO			B3	VREF0B3			F20			
IO			B3	VREF0B3	F17	H19	H19			
IO	DQ5T0		B3	VREF0B3	D16	B19	A20			
IO	DQ5T1		B3	VREF0B3	C16	C19	B20			
IO		DATA5	B3	VREF0B3	K18	F20	J19			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 38 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DQ5T2		B3	VREF0B3	E16	D19	C20			
IO	DQS5T		B3	VREF0B3	A16	C20	D20			
IO			B3	VREF0B3		G22	H20			
IO	DQ5T3		B3	VREF0B3	B16	E19	E20			
IO		DATA6	B3	VREF0B3	H18	F21	K19			
IO	DQ5T4		B3	VREF0B3	E17	A20	B21			
IO	DQ5T5		B3	VREF0B3	D17	B20	C21			
IO			B3	VREF1B3	F18	G21	G20			
IO	DQ5T6		B3	VREF1B3	B17	D20	D21			
IO			B3	VREF1B3			G21			
IO	DQ5T7		B3	VREF1B3	C17	E20	A22			
IO	RUP3		B3	VREF1B3	J18	F22	F21			
IO	RDN3		B3	VREF1B3	K19	F24	L19			
IO	DQ6T0		B3	VREF1B3	A18	B21	B22	DQ2T0	DQ1T0	
IO	DQ6T1		B3	VREF1B3	C18	C21	C22	DQ2T1	DQ1T1	
IO		DATA7	B3	VREF1B3	G18	G20	J20			
IO	DQ6T2		B3	VREF1B3	D18	A22	B23	DQ2T2	DQ1T2	
IO	DQS6T		B3	VREF1B3	B18	C22	D22	DQS2T		
IO			B3	VREF1B3		L19	L22			
IO	DQ6T3		B3	VREF1B3	A19	D21	C23	DQ2T3	DQ1T3	
IO		CLKUSR	B3	VREF1B3	J19	F23	H21			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 39 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DQ6T4		B3	VREF1B3	B19	E21	A24	DQ2T4	DQ1T4	
IO			B3	VREF1B3		J20	K20			
IO	DQ6T5		B3	VREF1B3	C19	B22	E22	DQ2T5	DQ1T5	
IO	DQ6T6		B3	VREF1B3	E19	D22	B24	DQ2T6	DQ1T6	
VREF1B3			B3	VREF1B3	E20	K19	E23			
IO	FCLK0		B3	VREF1B3	F19	E23	F22			
IO	FCLK1		B3	VREF1B3	G19	E25	G22			
IO	DQ6T7		B3	VREF1B3	D19	E22	D23	DQ2T7	DQ1T7	
IO			B3	VREF1B3	H19	H21	J21			
IO			B3	VREF1B3			K21			
IO	DQ7T0		B3	VREF1B3	B20	A23	D24	DQ2T8	DQ1T8	
IO	DQ7T1		B3	VREF1B3	A20	B23	A25	DQ2T9	DQ1T9	
IO	DQ7T2		B3	VREF1B3	C20	A24	C24	DQ2T10	DQ1T10	
IO			B3	VREF1B3			F23			
IO	DQS7T		B3	VREF1B3	D20	C24	B26		DQS1T	
IO	DQ7T3		B3	VREF1B3	A21	C23	B25	DQ2T11	DQ1T11	
IO			B3	VREF1B3	J20	H22	L23			
IO	DQ7T4		B3	VREF1B3	B21	D24	C25	DQ2T12	DQ1T12	
IO	DQ7T5		B3	VREF1B3	C21	B24	D25	DQ2T13	DQ1T13	
IO			B3	VREF1B3		J21	H22			
IO	DQ7T6		B3	VREF1B3	D21	D23	A26	DQ2T14	DQ1T14	

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 40 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DQ7T7		B3	VREF1B3	E21	E24	E24	DQ2T15	DQ1T15	
IO			B3	VREF1B3	H20	G23	K22			
GND			B3							
GND			B3							
GND			B3		G20	D28	H24			
IO			B3	VREF2B3			G23			
IO	DQ8T0		B3	VREF2B3	B22	A25	C26	DQ3T0	DQ1T16	
IO	DQ8T1		B3	VREF2B3	A22	C25	A28	DQ3T1	DQ1T17	
IO			B3	VREF2B3		F25	J22			
IO	DQ8T2		B3	VREF2B3	C22	B25	A27	DQ3T2	DQ1T18	
IO	DQS8T		B3	VREF2B3	D23	C26	B27	DQS3T		
IO			B3	VREF2B3			F24			
IO	DQ8T3		B3	VREF2B3	D22	D25	D26	DQ3T3	DQ1T19	
IO	DQ8T4		B3	VREF2B3	A23	A26	C27	DQ3T4	DQ1T20	
IO			B3	VREF2B3		E27	K23			
IO	DQ8T5		B3	VREF2B3	C23	B26	B28	DQ3T5	DQ1T21	
IO	DQ8T6		B3	VREF2B3	E23	E26	D27	DQ3T6	DQ1T22	
VREF2B3			B3	VREF2B3	E22	K20	E25			
IO	DQ8T7		B3	VREF2B3	B23	D26	E26	DQ3T7	DQ1T23	
IO			B3	VREF2B3	F20	J22	H23			
IO			B3	VREF2B3			J23			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 41 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
IO	DQ9T0		B3	VREF2B3	A24	B27	A29	DQ3T8	DQ1T24	
IO			B3	VREF2B3			L24			
IO	DQ9T1		B3	VREF2B3	C25	C27	B29	DQ3T9	DQ1T25	
IO			B3	VREF2B3	F21	H23	G24			
IO	DQ9T2		B3	VREF2B3	A25	A27	B30	DQ3T10	DQ1T26	
IO	DQS9T		B3	VREF2B3	C24	B28	C28			
IO			B3	VREF2B3	G21	C30	F25			
IO	DQ9T3		B3	VREF2B3	D24	D27	C29	DQ3T11	DQ1T27	
IO			B3	VREF2B3	G22	L21	J24			
IO	DQ9T4		B3	VREF2B3	B24	A28	D29	DQ3T12	DQ1T28	
IO	DQ9T5		B3	VREF2B3	B25	C28	D28	DQ3T13	DQ1T29	
IO	DQ9T6		B3	VREF2B3	A26	C29	C30	DQ3T14	DQ1T30	
IO			B3	VREF2B3	F22	E28	F26			
IO	DQ9T7		B3	VREF2B3	B26	B29	E28	DQ3T15	DQ1T31	
IO			B3	VREF2B3			K24			
VCCIO2					B28	C31	C31			
VCCIO2					M28	N31	C32			
VCCIO2					P20	T23	M32			
VCCIO2							T23			
VCCIO1					R20	U20	AA32			
VCCIO1					U28	W31	AK31			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 42 of 52)

Device					Package					
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA	DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
VCCIO1					AG28	AJ31	AK32			
VCCIO1							U23			
VCCIO8					Y15	AL29	AC17			
VCCIO8					AH17	AL19	AM21			
VCCIO8					AH27	Y17	AM30			
VCCIO7					Y14	AC16	AC16			
VCCIO7					AH2	AL13	AM12			
VCCIO7					AH12	AL3	AM3			
VCCIO6					R9	AJ1	AA1			
VCCIO6					U1	W1	AK1			
VCCIO6					AG1	U12	AK2			
VCCIO6							U10			
VCCIO5					B1	T9	C1			
VCCIO5					M1	N1	C2			
VCCIO5					P9	C1	M1			
VCCIO5							T10			
VCCIO4					A2	A3	A12			
VCCIO4					A12	A13	A3			
VCCIO4					J14	J16	K16			
VCCIO3					A17	M17	A21			
VCCIO3					A27	A19	A30			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 43 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
VCCIO3					J15	A29	K17			
VCCINT					M14	AA12	M12			
VCCINT					N11	AA14	M14			
VCCINT					N13	AA20	M19			
VCCINT					N15	L13	M21			
VCCINT					N17	L20	N13			
VCCINT					P12	M11	N15			
VCCINT					P14	M13	N18			
VCCINT					P16	M15	N20			
VCCINT					R13	M19	P12			
VCCINT					R15	M21	P14			
VCCINT					R17	N12	P16			
VCCINT					T12	N14	P17			
VCCINT					T14	N16	P19			
VCCINT					T16	N18	P21			
VCCINT					T18	N20	R13			
VCCINT					U11	P11	R15			
VCCINT					U13	P13	R18			
VCCINT					U15	P14	R20			
VCCINT					U17	P15	T14			
VCCINT					V12	P17	T16			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 44 of 52)

Device					Package					
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA	DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
VCCINT					V16	P19	T17			
VCCINT						P21	T19			
VCCINT						R12	U14			
VCCINT						R13	U16			
VCCINT						R14	U17			
VCCINT						R18	U19			
VCCINT						R19	V13			
VCCINT						R20	V15			
VCCINT						T11	V18			
VCCINT						T13	V20			
VCCINT						T19	W14			
VCCINT						T21	W16			
VCCINT						U10	W17			
VCCINT						U14	W19			
VCCINT						U18	Y13			
VCCINT						U22	Y15			
VCCINT						V11	Y18			
VCCINT						V13	Y20			
VCCINT						V15				
VCCINT						V17				
VCCINT						V19				

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 45 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
VCCINT						V21				
VCCINT						W12				
VCCINT						W14				
VCCINT						W16				
VCCINT						W18				
VCCINT						W20				
VCCINT						Y11				
VCCINT						Y13				
VCCINT						Y15				
VCCINT						Y19				
VCCINT						Y21				
GND					A14	A1	A10			
GND					A15	A11	A2			
GND					AA16	A2	A23			
GND					AC15	A21	A31			
GND					AF26	A30	AA16			
GND					AF3	A31	AA17			
GND					AG2	AA17	AC1			
GND					AG27	AA18	AC32			
GND					AH14	AB16	AD17			
GND					AH15	AD18	AF17			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 46 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
GND					B2	AK1	AL1			
GND					B27	AK2	AL2			
GND					C26	AK30	AL31			
GND					C3	AK31	AL32			
GND					G15	AL1	AM10			
GND					H16	AL11	AM2			
GND					L14	AL2	AM23			
GND					L15	AL21	AM31			
GND					M15	AL30	B1			
GND					N12	AL31	B2			
GND					N14	B1	B31			
GND					N16	B2	B32			
GND					N18	B30	H18			
GND					P1	B31	J17			
GND					P11	H17	K1			
GND					P13	H18	K32			
GND					P15	K16	M13			
GND					P17	L15	M15			
GND					P18	L17	M16			
GND					P28	M1	M17			
GND					R1	M12	M18			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 47 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
GND					R11	M14	M20			
GND					R12	M16	N12			
GND					R14	M18	N14			
GND					R16	M20	N16			
GND					R18	M31	N17			
GND					R28	N11	N19			
GND					T11	N13	N21			
GND					T13	N15	P13			
GND					T15	N17	P15			
GND					T17	N19	P18			
GND					U12	N21	P20			
GND					U14	P12	R14			
GND					U16	P16	R16			
GND					U18	P18	R17			
GND					V13	P20	R19			
GND					V14	R11	T12			
GND					V15	R15	T13			
GND					V17	R17	T15			
GND						R21	T18			
GND						T10	T20			
GND						T12	T21			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 48 of 52)

Device					Package					
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA	DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
GND						T14	U12			
GND						T18	U13			
GND						T20	U15			
GND						T22	U18			
GND						U11	U20			
GND						U13	U21			
GND						U15	V14			
GND						U17	V16			
GND						U19	V17			
GND						U21	V19			
GND						V12	W13			
GND						V14	W15			
GND						V16	W18			
GND						V18	W20			
GND						V20	Y14			
GND						W11	Y16			
GND						W13	Y17			
GND						W15	Y19			
GND						W17				
GND						W19				
GND						W21				

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 49 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
GND						Y1				
GND						Y12				
GND						Y14				
GND						Y16				
GND						Y18				
GND						Y20				
GND						Y31				
No connection					AC25	AA22	AA11			
No connection					AC26	AB10	AA13			
No connection					AC3	AB11	AB10			
No connection					AC4	AB15	AB12			
No connection					AD25	AB18	AC11			
No connection					AD26	AB19	AD10			
No connection					AD3	AC14	AD11			
No connection					AD4	AC15	AE10			
No connection					D25	AD14	AE16			
No connection					D26	H14	AE22			
No connection					D3	H15	AF11			
No connection					D4	J14	AF16			
No connection					E25	J15	AG16			
No connection					E26	K13	AG25			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 50 of 52)

Device					Package					
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA	DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
No connection					E3	K14	AG26			
No connection					E4	K21	AG27			
No connection						K22	AG28			
No connection						L10	AG5			
No connection						P22	AG7			
No connection						V10	AG8			
No connection							AH1			
No connection							AH16			
No connection							AH2			
No connection							AH21			
No connection							AH29			
No connection							AH31			
No connection							AH32			
No connection							AH4			
No connection							AH6			
No connection							E12			
No connection							E16			
No connection							E17			
No connection							E27			
No connection							E29			
No connection							E4			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 51 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
No connection							F11			
No connection							F28			
No connection							F5			
No connection							G11			
No connection							H10			
No connection							H15			
No connection							H16			
No connection							J10			
No connection							K10			
No connection							L10			
No connection							M11			
No connection							N11			
No connection							N22			
No connection							P11			
No connection							P22			
No connection							U22			
No connection							V12			
No connection							V22			
No connection							W11			
No connection							W12			
No connection							W21			

Table 4–1. Pin List for the Stratix EP1S30 Device (Part 52 of 52)

Device					Package			DQS for x16	DQS for x32	DIFFIO Speed *Note (1)*
Pad Name / Function	Optional Function(s)	Configuration Function	Bank Number	VREF Group	780-Pin FineLine BGA	956-Pin BGA	1020-Pin FineLine BGA			
No connection							W22			
No connection							Y11			
No connection							Y12			
No connection							Y21			
No connection							Y22			

Note to Table 4–1:

(1) The wire bond and flip-chip packages have different data rates for the high speed differential I/O channels. Table 4–2 shows the data rates as supported for each package.

Table 4–2. High Speed Differential I/O Channel Data Rates

Package	Package Type	High Speed Differential I/O Channel Performance (DIFFIO Speed)		Units
		High	Low	
780-pin FineLine BGA	flip chip	840	N/A	Mbps
956-pin BGA	flip chip	840	N/A	Mbps
1020-pin FineLine BGA	flip chip	840	462	Mbps

Pin Definitions

Table 4–3 shows pin definitions for the EP1S30 device.

Table 4–3. Pin Definitions for the EP1S30 Device (Part 1 of 5)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
Supply and Reference Pins		
VREF[1..4]B[1..8]	Input	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All of the VREF pins within a bank are shorted together. Each VREF pin can support up to 20 inputs on each side. If VREF pins are not used, designers should connect them to either VCC or Gnd.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards.
VCC_PLL5_OUTA	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9.
VCC_PLL5_OUTB	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10.
VCC_PLL6_OUTA	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11.
VCC_PLL6_OUTB	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12.
VCCA_PLL[1..12]	Power	Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..12]	Ground	Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
VCCG_PLL[1..12]	Power	Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDG_PLL[1..12]	Ground	Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.

Table 4–3. Pin Definitions for the EP1S30 Device (Part 2 of 5)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
Dedicated & Configuration/JTAG Pins		
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input	Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration.
nIO_PULLUP	Input	IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V.
PORSEL	Input	Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms.
VCCSEL	Input	VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA.
nCE	Input	Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.

Table 4–3. Pin Definitions for the EP1S30 Device (Part 3 of 5)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
TDO	Output	This is a dedicated JTAG input pin.
TRST	Input	This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit.
MSEL[2..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
Clock and PLL Pins		
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
FCLK[7..0]	Bidirectional	Optional fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins.
FPLL[10..7]CLKp	Input	Dedicated global clock inputs for fast PLLs (PLLs 7 through 10).
FPLL[10..7]CLKn	Input	Dedicated negative terminal associated with FPLL[10..7]CLKp pins.
CLK[15..0]p	Input	Dedicated global clock inputs 0 to 15.
CLK[15..0]n	I/O, Input	Optional negative terminal input for differential global clock input.
PLL6_OUT[3..0]p	I/O, Output	Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6).
PLL6_OUT[3..0]n	I/O, Output	Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL5_OUT[3..0]p	I/O, Output	Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5).

Table 4–3. Pin Definitions for the EP1S30 Device (Part 4 of 5)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PLL5_OUT[3..0]n	I/O, Output	Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
Optional/Dual-Purpose Pins		
DATA0	I/O, Input	Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete.
DIFFIO_TX[0..151]n	I/O, Output	This pin can be used as the complementary signal of the differential inputs and outputs. If not used for the differential pair, these pins are regular I/O pins. Pins with an n suffix carry the negative signal for the differential channel. Pins with a p suffix carry the positive signal for the differential channel.
PLL5_FBp	I/O, Input	External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used.
PLL5_FBn	I/O, Input	Negative terminal input for external feedback input PLL5_FBp.
PLL6_FBp	I/O, Input	External feedback input pin for PLL6.
PLL6_FBn	I/O, Input	Negative terminal input for external feedback input PLL6_FBp.
INIT_DONE	I/O, Output	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
DATA[7..1]	I/O, Input	Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.

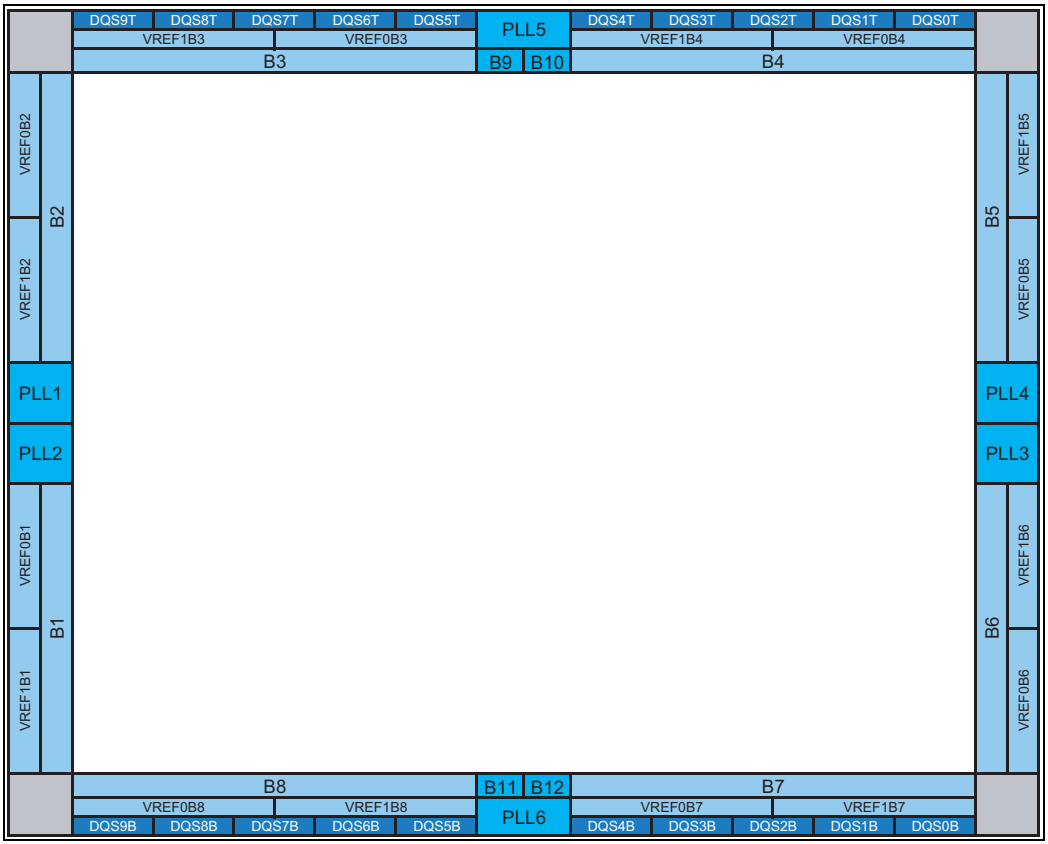
Table 4–3. Pin Definitions for the EP1S30 Device (Part 5 of 5)

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration
nCS,CS	I/O, Input	These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins.
RUP[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{UP} must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins.
RDN[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors RDN must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins.
RUnLU	I/O, Input	Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2 = 0, the RUnLU pin is a user I/O pin.

PLL & Bank Diagram

Figure 4–1 shows the PLL and bank locations for the EP1S30 device.

Figure 4–1. PLL and Bank Diagram *Notes (1), (2)*



Notes for Figure 4–1:

(1) This is a top view of the silicon die. For flip chip packages the die is mounted upside down in the package.

(2) This is a pictoral representation only, to give an idea of placement on the device. Refer to the pinlist and the Quartus II software for exact locations.

Fast PLL to High-Speed I/O Connections

Table 4–4 shows the number of high-speed differential I/O channels that can be driven by each Fast PLL for the EP1S30 device..

Table 4–4. Clock Resources for High Speed Differential I/O (DIFFIO) Receiver and Transmitter channels. Notes (5),(7)

Device	Pin Count	Source FAST PLL	Rx Channels (1)		Tx channels (2)		Overlapped Rx Channels (3)		Overlapped Tx Channels (4)	
			High (6)	Low (6)	High (6)	Low (6)	High (6)	Low (6)	High (6)	Low (6)
EP1S30	780	PLL1	[20-36]	-	[21-38]	-	[21-36]	-	[21-38]	-
		PLL2	[4-19]	-	[3-19]	-	[4-19]	-	[3-19]	-
		PLL3	[62-77]	-	[62-78]	-	[62-77]	-	[62-78]	-
		PLL4	[45-61]	-	[43-60]	-	[45-60]	-	[43-60]	-
		PLL7	(8)	(8)	(8)	(8)	(8)	(8)	(8)	(8)
		PLL8	(8)	(8)	(8)	(8)	(8)	(8)	(8)	(8)
		PLL9	(8)	(8)	(8)	(8)	(8)	(8)	(8)	(8)
		PLL10	(8)	(8)	(8)	(8)	(8)	(8)	(8)	(8)
	956	PLL1	[20-39]	-	[21-39]	-	[21-39]	-	[21-39]	-
		PLL2	[0-19]	-	[0-19]	-	[0-19]	-	[0-19]	-
		PLL3	[62-81]	-	[62-81]	-	[62-81]	-	[62-81]	-
		PLL4	[42-61]	-	[42-60]	-	[42-60]	-	[42-60]	-
		PLL7	[21-39]	-	[21-40]	-	[21-39]	-	[21-39]	-
		PLL8	[0-19]	-	[0-19]	-	[0-19]	-	[0-19]	-
		PLL9	[62-81]	-	[62-81]	-	[62-81]	-	[62-81]	-
		PLL10	[42-60]	-	[41-60]	-	[42-60]	-	[42-60]	-
	1020	PLL1	[20-39]	-	[21-39]	-	[21-39]	-	[21-39]	-
		PLL2	[0-19]	-	[0-19]	-	[0-19]	-	[0-19]	-
		PLL3	[62-81]	-	[62-81]	-	[62-81]	-	[62-81]	-
		PLL4	[42-61]	-	[42-60]	-	[42-60]	-	[42-60]	-
		PLL7	[21-39]	[40]	[21-40]	[20]	[21-39]	-	[21-39]	-
		PLL8	[0-19]	-	[0-19]	-	[0-19]	-	[0-19]	-
		PLL9	[62-81]	-	[62-81]	-	[62-81]	-	[62-81]	-
		PLL10	[42-60]	[41]	[41-60]	[61]	[42-60]	-	[42-60]	-

Table 4–4. Clock Resources for High Speed Differential I/O (DIFFIO) Receiver and Transmitter channels. Notes (5),(7)

Device	Pin Count	Source FAST PLL	Rx Channels (1)		Tx channels (2)		Overlapped Rx Channels (3)		Overlapped Tx Channels (4)	
			High (6)	Low (6)	High (6)	Low (6)	High (6)	Low (6)	High (6)	Low (6)

Notes for Table 4–4:

(1) These Rx channels can be clocked by the PLL listed in the "FAST PLL Source location" column.

(2) These Tx channels can be clocked by the PLL listed in the "FAST PLL Source location" column.

(3) These Rx channels can be driven by the PLL listed in the "FAST PLL Source location" or alternatively be driven by the other adjacent FAST PLL. See the PLL & Bank Diagram for PLL locations.

(4) These Tx channels can be driven by the PLL listed in the "FAST PLL Source location" or alternatively be driven by the other adjacent FAST PLL. See the PLL & Bank Diagram for PLL locations.

(5) Each range of channel numbers are shown in [ ] brackets.

(6) Data channels designated as "high" speed support a maximum data rate of 840 Mbps for -5 and -6 speed grade devices and 624 Mbps for -7 speed grade devices. The -8 speed grade and data channels designated as "low" speed support a maximum data rate of 462 Mbps for all speed grades.

(7) The high speed differential I/O (DIFFIO) channels span across two banks on both sides of the device. Each Fast PLL can normally only feed channels in one bank. However, the center PLLs can also clock the channels associated with the adjacent center PLL on the same side of the device through a multiplexer that is shown in figures 5-16 and 5-17 in volume 2 of the Stratix Device Handbook. These channels are called "cross-bank" channels. When cross-bank channels are used only one center PLL on each side can be used.

(8) PLLs 7, 8, 9, and 10 are not available for the EP1S30 and EP1S40 devices in the F780 package.