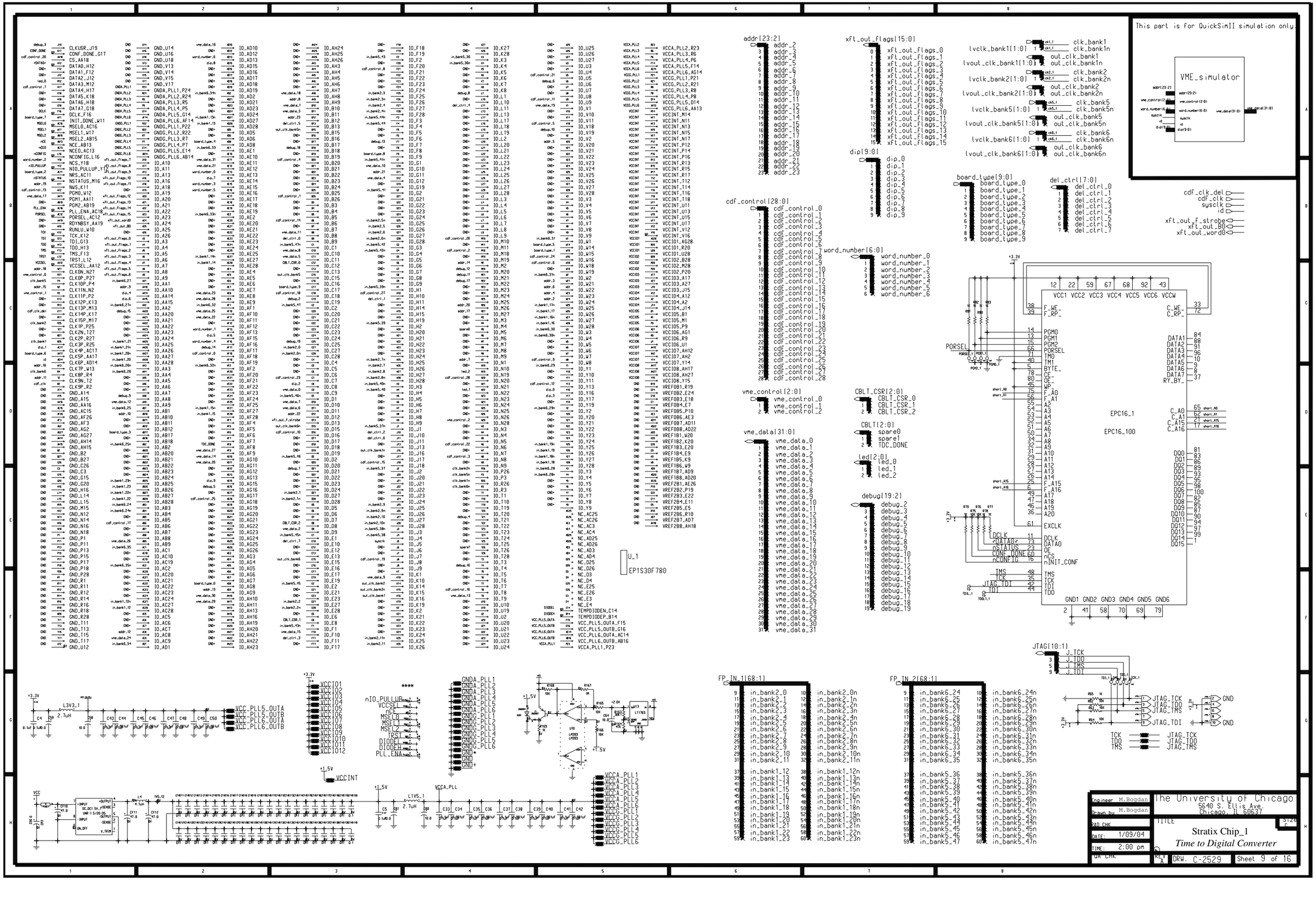
This part is for QuickSimII simulation only
VME_simulator
addr[23:2]
vme_control[2:0]
word_number[6:0]
sysclk
id
dip[9:0]
vme_data[31:0]
clk_bank1
clk_bank1n
clk_bank2
clk_bank2n
clk_bank5
clk_bank5n
clk_bank6
clk_bank6n
out_clk_bank1
out_clk_bank1n
out_clk_bank2
out_clk_bank2n
out_clk_bank5
out_clk_bank5n
out_clk_bank6
out_clk_bank6n
xft_out_flags[15:0]
board_type[9:0]
del_ctrl[7:0]
cdf_clk_del
cdf_clk
sysclk
id
xft_out_f_strobe
xft_out_B0
xft_out_word0
U_1
EP1S30F780
cdf_control[28:0]
vme_control[2:0]
vme_data[31:0]
CBLT_CSR[2:0]
CBLT[2:0]
led[2:0]
debug[19:2]
VCCA_PLL2_R23
VCCA_PLL3_R6
VCCA_PLL4_P6
VCCA_PLL5_F14
VCCA_PLL6_AG14
VCCG_PLL1_P21
VCCG_PLL2_R21
VCCG_PLL3_R8
VCCG_PLL4_P8
VCCG_PLL5_D14
VCCG_PLL6_AA13
VCCINT_M14
VCCINT_N11
VCCINT_N13
VCCINT_N15
VCCINT_N17
VCCINT_P12
VCCINT_P14
VCCINT_P16
VCCINT_R13
VCCINT_R15
VCCINT_R17
VCCINT_T12
VCCINT_T14
VCCINT_T16
VCCINT_T18
VCCINT_U11
VCCINT_U13
VCCINT_U15
VCCINT_U17
VCCINT_V12
VCCINT_V16
VCCIO1_AG28
VCCIO1_R20
VCCIO1_U28
VCCIO2_B28
VCCIO2_M28
VCCIO2_P20
VCCIO3_A17
VCCIO3_A27
VCCIO3_J15
VCCIO4_A12
VCCIO4_A2
VCCIO4_J14
VCCIO5_B1
VCCIO5_M1
VCCIO5_P9
VCCIO6_AG1
VCCIO6_R9
VCCIO6_U1
VCCIO7_AH12
VCCIO7_AH2
VCCIO7_Y14
VCCIO8_AH17
VCCIO8_AH27
VCCIO8_Y15
VREFB01_R19
VREFB02_E24
VREFB03_E18
VREFB04_E7
VREFB05_P10
VREFB06_AE3
VREFB07_AD11
VREFB08_AD22
VREFB1_W20
VREFB2_K20
VREFB3_E22
VREFB4_E11
VREFB5_E5
VREFB6_R10
VREFB7_AD7
VREFB8_AH18
VCCA_PLL1_P23
VCCG_PLL6_OUTB_AB16
VCCG_PLL5_OUTB_G16
VCCG_PLL5_OUTA_AC14
VCC_PLL5_OUTA_F15
TEMPDIODEP_B14
TEMPDIODEN_C14
FP_IN_1[68:1]
FP_IN_2[68:1]
JTAG[10:1]
JTAG_TCK
JTAG_TDO
JTAG_TMS
JTAG_TDI
GND
VCCIO1
VCCIO2
VCCIO3
VCCIO4
VCCIO5
VCCIO6
VCCIO7
VCCIO8
VCCIO9
VCCIO10
VCCIO11
VCCIO12
VCC_PLL5_OUTA
VCC_PLL5_OUTB
VCC_PLL6_OUTA
VCC_PLL6_OUTB
VCCINT
VCCA_PLL
VCCA_PLL1
VCCA_PLL2
VCCA_PLL3
VCCA_PLL4
VCCA_PLL5
VCCA_PLL6
VCCG_PLL1
VCCG_PLL2
VCCG_PLL3
VCCG_PLL4
VCCG_PLL5
VCCG_PLL6
GNDA_PLL1
GNDA_PLL2
GNDA_PLL3
GNDA_PLL4
GNDA_PLL5
GNDA_PLL6
GNDG_PLL1
GNDG_PLL2
GNDG_PLL3
GNDG_PLL4
GNDG_PLL5
GNDG_PLL6
nIO_PULLUP
VCCSEL
nCE
MSEL0
MSEL1
MSEL2
TRST
DIODEP
DIODEN
PLL_ENA
Engineer M.Bogdan
Drawn by M.Bogdan
PAD CHK
DATE: 1/09/04
TIME: 2:00 pm
QA CHK
The University of Chicago
5640 S. Ellis Ave.
Chicago, IL 60637
TITLE
Stratix Chip_1
Time to Digital Converter
Size C
REV A
DRW. C-2529
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