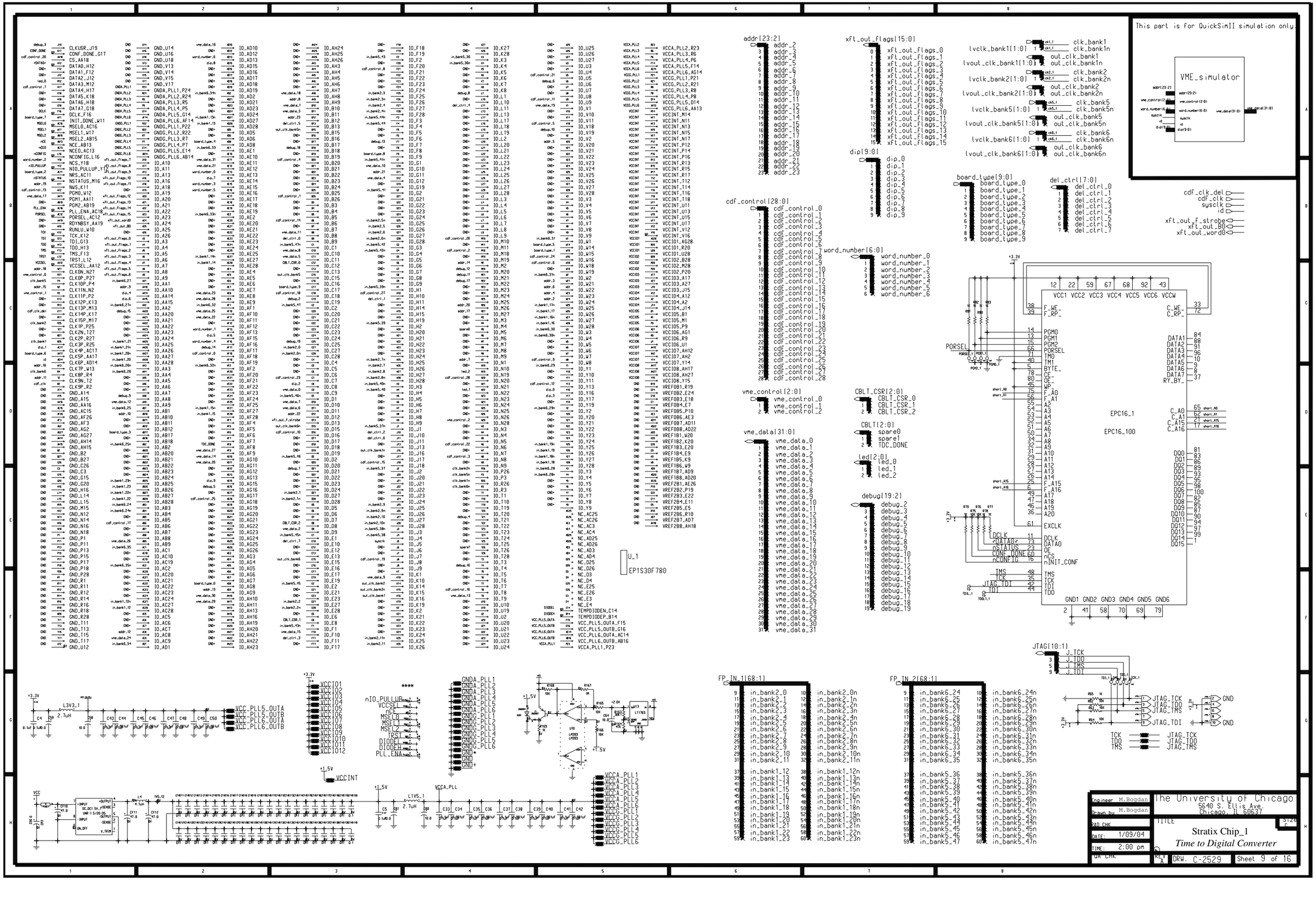
This part is for QuickSimII simulation only.
VME_simulator
addr[23:2]
xft_out_flags[15:0]
dip[9:0]
cdf_control[28:0]
word_number[6:0]
board_type[9:0]
del_ctrl[7:0]
vme_control[2:0]
vme_data[31:0]
CBLT_CSR[2:0]
CBLT[2:0]
led[2:0]
debug[19:2]
JTAG[10:1]
FP_IN_1[68:1]
FP_IN_2[68:1]
EP1S30F780
EPC16_1
EPC16_100
VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCCW
GND1 GND2 GND3 GND4 GND5 GND6
Engineer M.Bogdan
Drawn by M.Bogdan
RAD CHK
DATE: 1/09/04
TIME: 2:00 pm
QA CHK
The University of Chicago
5640 S. Ellis Ave.
Chicago, IL 60637
TITLE
Stratix Chip_1
Time to Digital Converter
Size C
REV A
DRW. C-2529
Sheet 9 of 16