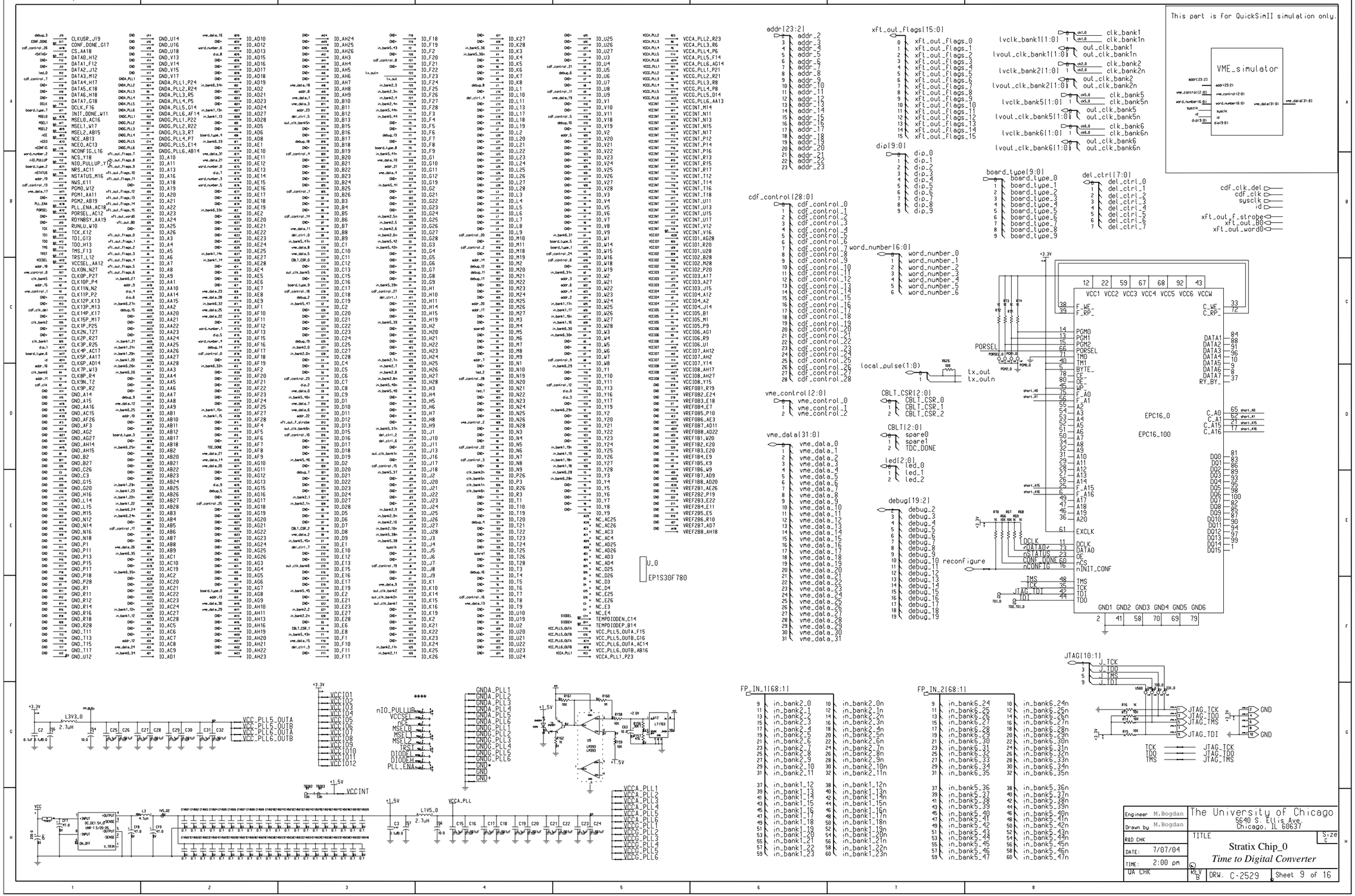
This part is for QuickSimII simulation only.
VME_simulator
addr[23:2]
vme_control[2:0]
word_number[6:0]
sysclk
id
dip[3:0]
vme_data[31:0]
clk_bank1
clk_bank1n
out_clk_bank1
out_clk_bank1n
clk_bank2
clk_bank2n
out_clk_bank2
out_clk_bank2n
clk_bank5
clk_bank5n
out_clk_bank5
out_clk_bank5n
clk_bank6
clk_bank6n
out_clk_bank6
out_clk_bank6n
cdf_clk_del
cdf_clk
sysclk
id
xfut_out_f_strobe
xfut_out_B0
xfut_out_word0
addr[23:2]
xfut_out_flags[15:0]
dip[9:0]
board_type[9:0]
del_ctrl[7:0]
cdf_control[28:0]
word_number[6:0]
local_pulse[1:0]
CBLT_CSR[2:0]
CBLT[2:0]
led[2:0]
debug[19:2]
reconfigure
U_0
EP1S30F780
VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCCW
PORSEL
EPC16_0
EPC16_100
JTAG[10:1]
TCK
TDO
TMS
JTAG_TCK
JTAG_TDO
JTAG_TMS
JTAG_TDI
GND
FP_IN_1[68:1]
FP_IN_2[68:1]
VCCINT
VCCA_PLL
L3V3_0
L1V5_0
Engineer M.Bogdan
Drawn by M.Bogdan
R&D CHK
DATE: 7/07/04
TIME: 2:00 pm
UA CHK
The University of Chicago
5640 S. Ellis Ave.
Chicago, IL 60637
TITLE
Stratix Chip_0
Time to Digital Converter
Size C
REV B
DRW. C-2529
Sheet 9 of 16