# A New Time-to-Digital Converter for the Central Tracker of the Colliding Detector at Fermilab

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*Abstract*-- **We describe a FPGA-based, 96-channel, time-to-digital converter (TDC) intended for use with the Central Outer Tracker (COT) in the CDF experiment at the Fermilab Tevatron. The COT system is digitized and read out by 315 TDC cards, each serving 96 wires of the chamber. The TDC, which is implemented as a 9U VME card, has been built around two Altera Stratix FPGAs. The special capabilities of this device are the availability of 840MHZ LVDS inputs, multiple phase locked clock modules, and abundant memory. The TDC system would operate with an input resolution of 1.2ns, a minimum input pulse width of 4.8ns and a minimum separation of 4.8ns between pulses. Each wire input can accept up to 7 hits per collision. Memory pipelines are included for each channel to allow deadtimeless operation in the first-level trigger; the pipeline has a depth of 5.5us to allow the data to pass into one of four separate level-two buffers for readout. If the level-two buffer is accepted, the data are passed through a processor implemented in the FPGA to encode the relative time-to-digital values by using the memory positions and addresses of the transitions due to the input pulses. This processing and moving of the data takes 12 microseconds; the results are then loaded into an output VME memory. A separate memory contains the resulting word count, which is used in performing a VME 64-bit Chain Block Transfer of an entire sixteen-card crate. The TDC must also produce prompt trigger flags for a tracking trigger processor called the Extremely Fast Tracker (XFT). This separate path uses the same input data but passes the stream through a special processor, also implemented in the FPGA, to develop the trigger data delivered with a 22ns clock to the XFT through a high-speed transmission cable assembly. The full TDC design and multi-card test results will be described.**

## I. INTRODUCTION

$T$he Collider Detector at Fermilab (CDF), is a large (5000-ton) detector of particles produced in proton-antiproton collisions at 1.96 TeV at the Fermilab Tevatron. The detector consists of a solenoidal magnetic spectrometer surrounded by systems of segmented calorimeters and muon chambers. Inside the solenoid, precision tracking systems measure the trajectories of particles; the particle momenta are measured from the curvature in the magnetic field and the energy deposited in the calorimeters. The tracking systems consist of a silicon-strip system with >750,000 channels around the beam-pipe, followed by the Central Outer Tracker (COT), a large cylindrical drift chamber with 30,240 sense wires arranged in 96 layers divided into 8 "superlayers" of 12 wires each. Four of the layers have the wires parallel to the beam axis; the remaining four are tilted by +- 3 degrees to provide small-angle stereo for 3D reconstruction of tracks. The maximum drift time of the COT is ~200 nsec; the maximum drift length is 0.88 cm.

During the present Run II, the peak luminosity of the Tevatron has grown to well over $10^{32}$ , a factor of more than five higher than in Run I. The Tevatron operates with 396 nsec bunch spacing, with the result that the occupancy (hits/channel) in the COT increases with luminosity as the number of proton-antiproton collisions per beam crossing is now greater than one. The increased occupancy puts a load on the rate at which CDF can record events to permanent media. While CDF is operating at its design readout bandwidth, there are still more good events than can presently be logged, particularly due to the success of the Silicon Vertex Trigger (SVT), which has given us a new capability to trigger on events from b-quarks. A broad range of efforts are underway to upgrade the readout bandwidth to allow operation at

luminosities up to $3 \times 10^{32}$ , including the development of a new time-to-digital converter (TDC) for the COT.

In this note we describe the design of a new TDC for the COT based entirely on FPGAs. Four working prototypes have been built and tested. Thirty-five preproduction boards have been ordered for full-crate tests this summer. A suite of test routines has been implemented, and a custom test card with 96 independently controlled output channels is under construction.

## II. PRINCIPLE OF OPERATION

The principle of the Time-to-Digital conversion is presented in Figure 1, as seen in the Quartus II [1] simulation window. The incoming LVDS signal is applied to a dedicated input pin, serdes_in, of an Altera Stratix [2] FPGA. An internal megafunction implements the deserialization receiver.
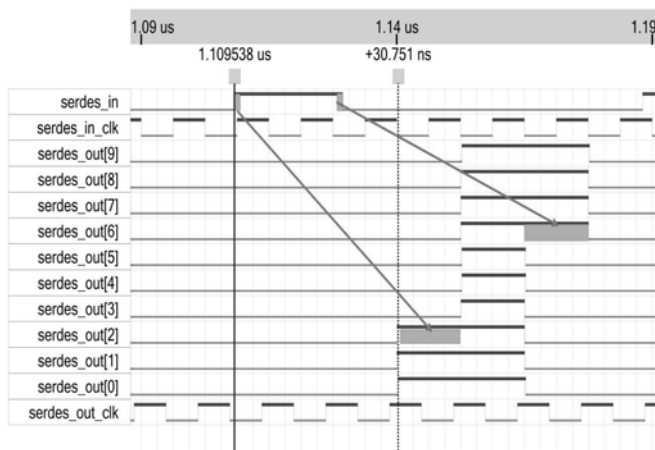


Fig. 1. Principle of operation.

The input pulse is converted into a 10-bit data stream, serdes_out[9..0], moving on a 12ns clock period. The leading edge is determined by counting the number of "0" bits before the first "1" bit of a string of at least four "1" bits. The pulse width is calculated by counting the number of successive bits until a string of at least four "0" bits occurs.

## III. TDC BOARD – BLOCK DIAGRAM

The block diagram and the data flow on the board are presented in Figure 2.

This entire card has been built around two Altera STRATIX FPGAs: TDC Chip_0 and TDC Chip_1, which have identical designs.

The TDC Board is designed to function in existing standard CDF Readout Crates and uses specific backplane signals [3] generated by the CDF Trigger System Interface, Tracer and Master Clock.

On the front panel, the board has 96 differential inputs, 48 for each TDC Chip, and receives pulses from the COT. The signals are first applied to a repeater block. The midpoint voltage of +1.25Vcc is generated with a linear regulator from the +5Vcc power supply. The repeater converts the COT signals into standard LVDS and passes them directly to the TDC chips.

The two TDC Chips receive the COT pulses and generate the Hit-Count and Hit-Data results in the internal VME Readout buffers.

Trigger flags used by the eXtremely Fast Tracker (XFT) to identify tracks in the COT are also generated and sent out via the backplane connector P3 through a set of tri-state buffers.

The VME interface block is also implemented with an Altera FPGA. It coordinates VME access to the TDC Chips for regular and Chain Block Transfers (CBLT) [4] in both 32-bit and 64-bit modes. The VME Chip itself connects only to the 16 LSB of the VME data bus.

The 132ns CDF Clock from the backplane is first converted to TTL with a PECL receiver, then phase-locked, buffered and applied to the TDC Chips directly and also through a pair of programmable delay lines.

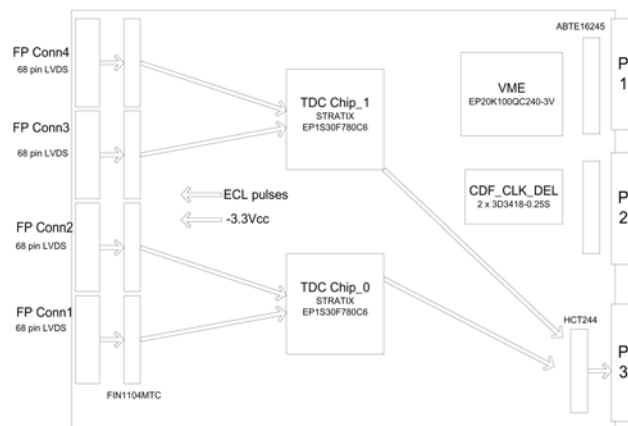Each FPGA on board is connected to a 20-pin header for logic analyzer hook-up.



Fig. 2. TDC Board - Block Diagram and Data flow.

## IV. TDC CHIP - BLOCK DIAGRAM

The block diagram of the TDC Chip is presented in Figure 3. The 48 LVDS inputs are applied directly to a deserialization block and converted into a 480-bit data bus.

Unwanted channels can be eliminated with a VME command [5], by controlling the MUX/MASK block. After a channel has been blocked out, the registers can be cleared via VME so that no residual "1" bits are passed along and detected as hits.

Upon a Level-1 Accept (L1A) trigger pulse, data pass through a 512x480 RAM, the Pipeline, and is written into one of the four Level-2 Buffers. The write and read addresses for the Pipeline come from the same, 9-bit, circular counter. The difference between those two values is controlled via VME and corresponds to the actual time difference between the L1A

pulse and the moment at which the signal that gets stored in the Level-2 Buffer reaches the TDC chip. The writing of each Level-2 Buffer is independent; therefore the chip accepts L1A pulses on each CDF clock edge. There is no data loss if one starts writing of a Level-2 Buffer before the writing of another one has ended. The number of words written in the Level-2 Buffer is set with a VME write command.

A Level-2 Accept (L2A) trigger pulse transfers data from the selected Level-2 Buffer into another, identical memory and then to the Edge Detector Block. The second RAM is required in order to free the Level-2 Buffer for a new L1A pulse.

The Edge Detector receives a stream of 10-bit words for each channel and detects hits by analyzing every bit, starting with MSB of the first word. One "0" bit, followed by four "1" bits is considered a leading edge. One "1" bit followed by four "0" bits, is considered a trailing edge.

If the 0->1 transition comes before the beginning of the time range, i.e. if the 4 MSBs of the first word in the Level-2 Buffer are "1", the leading edge is 0x00.

If the 1->0 transition comes after the end of the time range, i.e., if a leading edge is found but a trailing edge is not, 0xFF is written as pulse width.

A variable number of hits, up to a maximum of seven, can be detected for each channel.
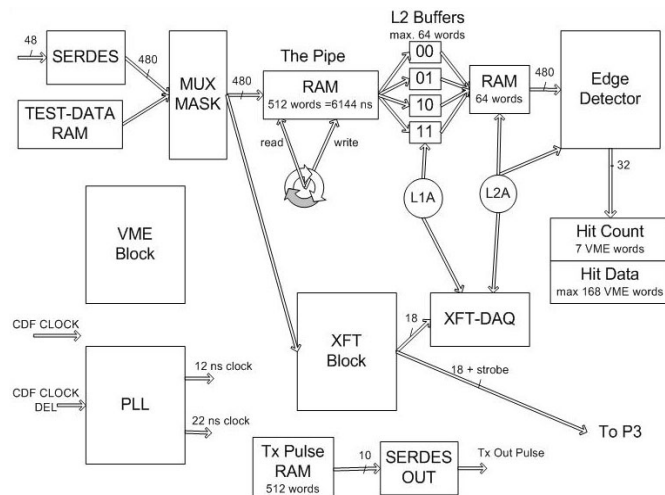


Fig. 3. TDC Chip - Block Diagram.

The Edge Detector block works in two basic steps. The first is finding and storing the edges on each of the 48 wires and the second is collecting and packing all the hit data together. Each wire has two eight-word RAMs associated with it used to store the leading edges and widths of the hits. Once all the words have been searched, the Edge Detector moves all the hit data words from the eight-word RAMs to two VME readout buffers, one for the number of hits and one for the actual hit data, as follows:

1. Hit-Count: 4 bits are used to present the number of hits. Bit 3 is the channel ON/OFF status and bits [2..0] are the actual number of hits. The number of Hit-Count words to read after a L2A pulse is: 4 bits/channel x 48 channels/chip + 1 header VME word = 7 VME words/chip;

2. Hit-Data: Each hit is recorded as a Leading Edge [7..0], Pulse Width [7..0] pair. The number of newly recorded hits varies after each L2A pulse; the maximum number of Hit-Data words to read after a L2A pulse is: 16 bits/hit x 7 hits/channel x 48 channels/chip = 168 VME words/chip.

Since the Hit-Data VME readout buffer is never cleared during normal operation; it may include hits from old events at higher addresses than the current hits occupy.

After each L2A pulse, the Edge Detector presents the number of new 32-bit Hit-Data words to the VME chip on board. The VME chip uses this information to control the Chain Block Transfer. The number of Hit-Data words may also be read out via VME for testing purposes.

The same data stream that enters the Pipeline is applied to the XFT block that generates the trigger flags used by the XFT.

The XFT block also connects to a dedicated DAQ system similar to the main one. It has the same Pipeline/Level-2 Buffers/VME-Readout Buffer structure and follows the same L1A/L2A sequence as the hit-data stream. The length of the XFT-Level-2 Buffers is also VME controlled. The XFT-DAQ is designed to be used for testing purposes only. Also for testing, the XFT block is fitted with another simple VME Readout RAM that contains the current XFT flags. This RAM can be frozen and read out via VME.

The PLL block generates the 12ns and 22ns clocks used inside the chip. All the clocks are in sync with the delayed CDF clock.

The regular, un-delayed, CDF clock is also received and used only to latch in the CDF-specific backplane signals.

The SERDES OUT block generates an LVDS pulse pattern, used for testing. The number of successive pulses and the timing is controlled via VME by writing the content of the Tx PULSE RAM.

## V. REFERENCES

[1] Altera Corporation, "Quartus II Handbook", ver.2.1, August 2004.
[2] Altera Corporation, "Stratix Device Handbook", ver.3.0, Apr. 2004.
[3] T. Shaw and G. Sullivan, "A Standard Front-End Trigger VME Bus Based Readout Crate for the CDF Upgrade", CDF/DOC/TRIGGER/CDFR/2388, May 12, 1998.
[4] ANSI/VITA 23-1998, Approved March 22, 1998.
[5] Mircea Bogdan and Harold Sanders, "Run IIB TDC-II Address Space", CDF Note 6998, ver.0.01, June 2004.