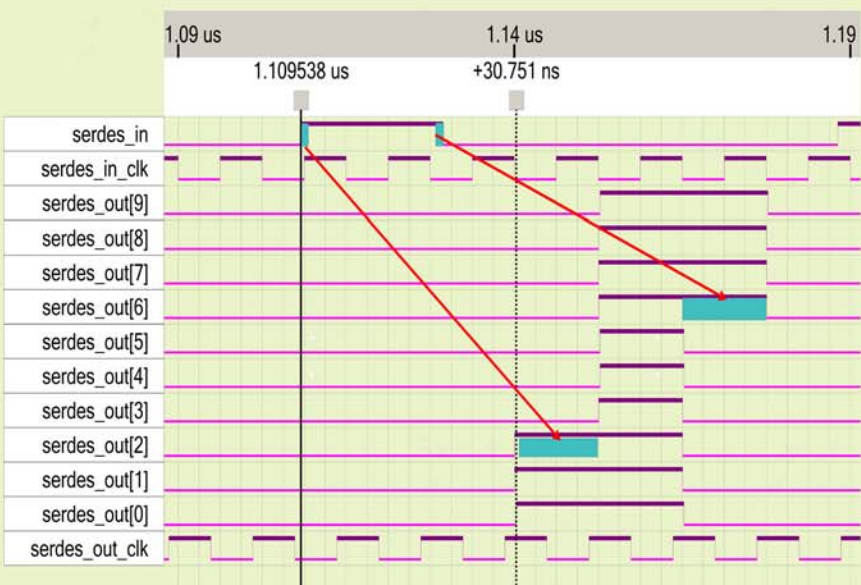
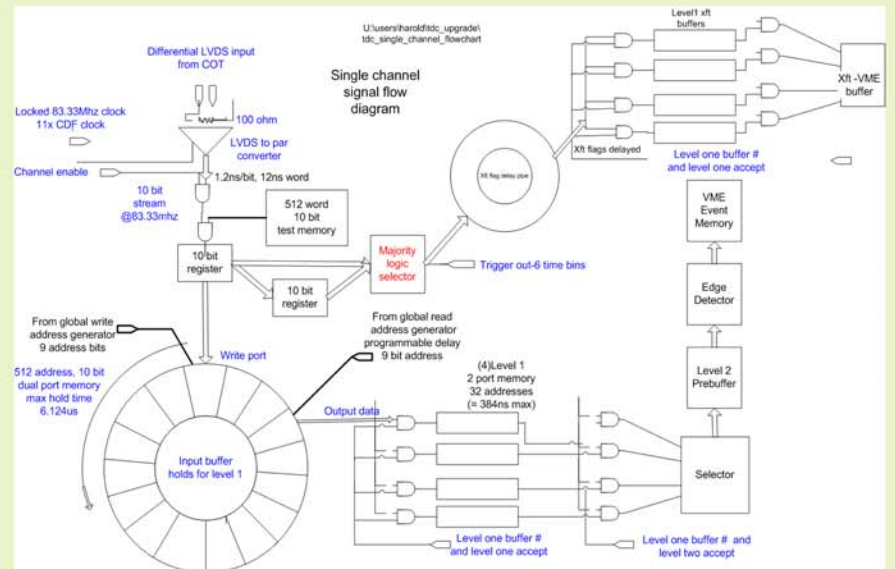


A New Time to Digital Converter for the Central Tracker of the Colliding Detector at Fermilab

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Abstract-- We describe a FPGA-based, 96-channel, time-to-digital converter (TDC) intended for use with the Central Outer Tracker (COT) in the CDF experiment at the Fermilab Tevatron. The COT system is digitized and read out by 315 TDC cards, each serving 96 wires of the chamber. The TDC, which is implemented as a 9U VME card, has been built around two Altera Stratix FPGAs. The special capabilities of this device are the availability of 840MHz LVDS inputs, multiple phase locked clock modules and abundant memory. The TDC system would operate with an input resolution of 1.2ns and a minimum input pulse width of 4.8ns, and a minimum separation of 4.8ns between pulses. Each wire input can accept up to 7 hits per collision. Memory pipelines are included for each channel to allow deadtimeless operation in the first-level trigger; the pipeline has a depth of 5.5us to allow the data to pass into one of four separate level-two buffers for readout. If the level-two buffer is accepted, the data are passed through a processor implemented in the FPGA to encode the relative time-to-digital values by using the memory positions and addresses of the transitions due to the input pulses. This processing and moving of the data takes seven microseconds; the results are then loaded into an output VME memory. A separate memory contains the resulting word count, which is used in performing a VME 64-bit Chain Block Transfer of an entire sixteen-card crate. The TDC must also produce prompt trigger flags for a tracking trigger processor called the Extremely Fast Tracker (XFT). This separate path uses the same input data but passes the stream through a special processor, also implemented in the FPGA, to develop the trigger data delivered with a 22ns clock to the XFT through a high-speed transmission cable assembly. The full TDC design and multi-card test results will be described.



TDC Single Channel Flow-Chart:

- LVDS pulse converted to a 10-bit data bus via SERDES Block;
- any channel can be blocked out with a VME command;
- data passes through a 512-word RAM (The Pipeline);
- the chip is fitted with a 4-buffer DAQ system;
- on L_1 trigger pulse, up to 64 words are written into one of four buffers;
- on L_2 trigger pulse, buffer content enters Edge Detector Block;
- hits are calculated and stored into VME Event Memory;
- in parallel, the XFT block generates the trigger flags used by the eXtremely Fast Tracker (XFT) to identify tracks in the Central Outer Tracker (COT);
- the XFT trigger flags are sent downstream via backplane connector P3;
- the XFT block has also a 4-buffer DAQ system for testing.

Principle of the Time to Digital conversion, seen in the QuartusII simulation window:

- incoming LVDS pulse is applied to input pin of Altera Stratix FPGA;
- pulse is deserialized into a 10-bit data stream, with a 12ns clock period;
- leading edge is determined by the number of bits before the first "1" bit of a string of at least four successive "1" bits;
- pulse width is calculated by counting the number of successive bits until a string of at least four "0" bits occurs.

TDC Board features:

- single-width, 9U x 400 mm VME standard module;
- board built around two Altera Stratix FPGAs: EP1S30F780C6;
- 48 LVDS input channels per Chip (96Channels/Board);
- input resolution of 1.2ns;
- minimum pulse width of 4.8ns and 4.8ns between pulses;
- max. 7 hits per collision for each wire;
- first trigger level latency adjustable to 5.5 us;
- four separate level-two buffers with adjustable depth;
- 10us for the result to be calculated and loaded in the output buffers;
- VME read-out: 32-bit or 64-bit CBLT;
- board generates trigger flags for a downstream tracking processor;
- power used: +5V/ 10A and -5V/ 0.5A from backplane;
- board generates: +2.5V/3A, +3.3V/15A, +1.5V/20A and -3.3V/1.5A.

