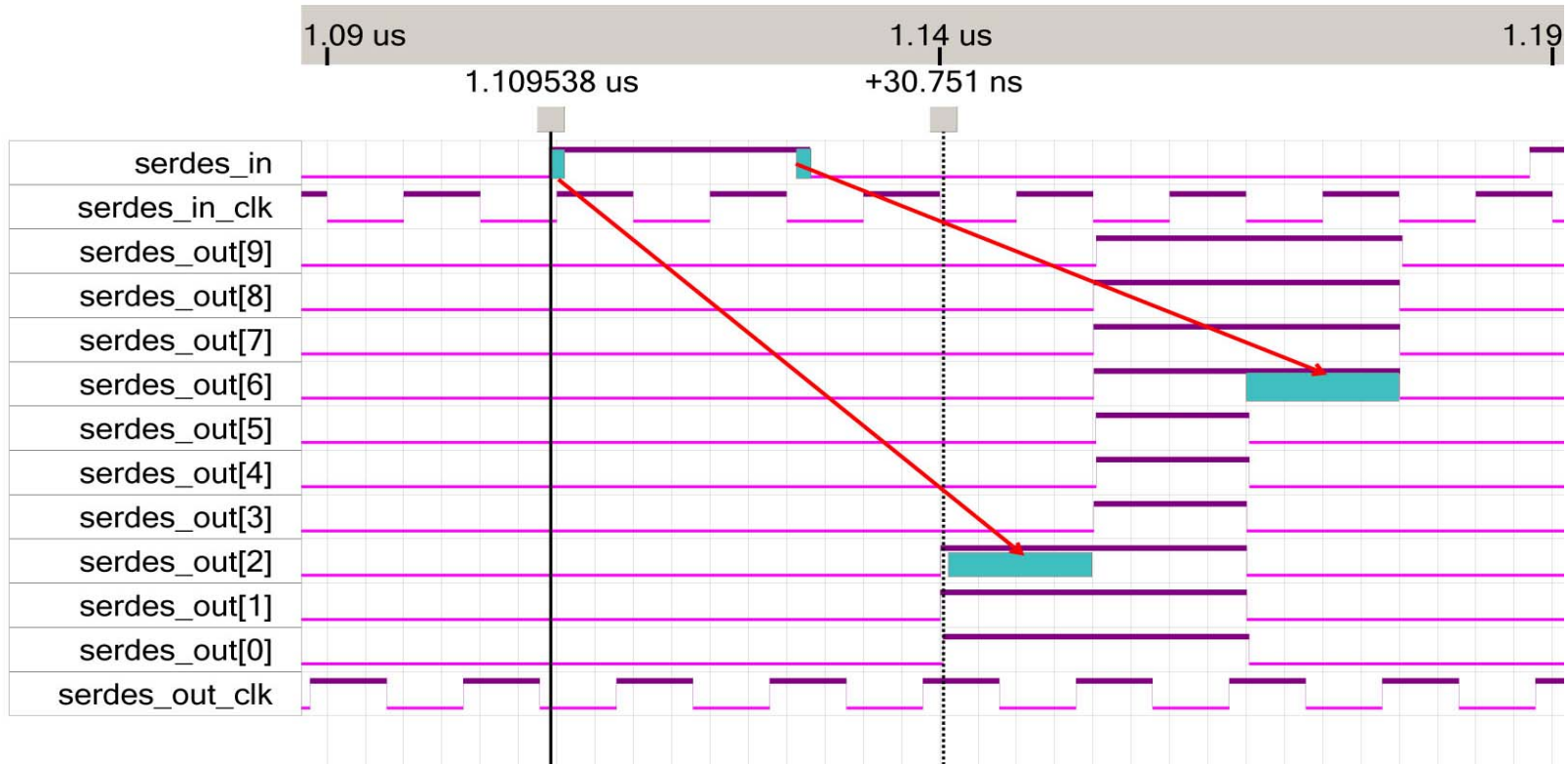


Chicago TDC Design and Implementation

Mircea Bogdan (UC)

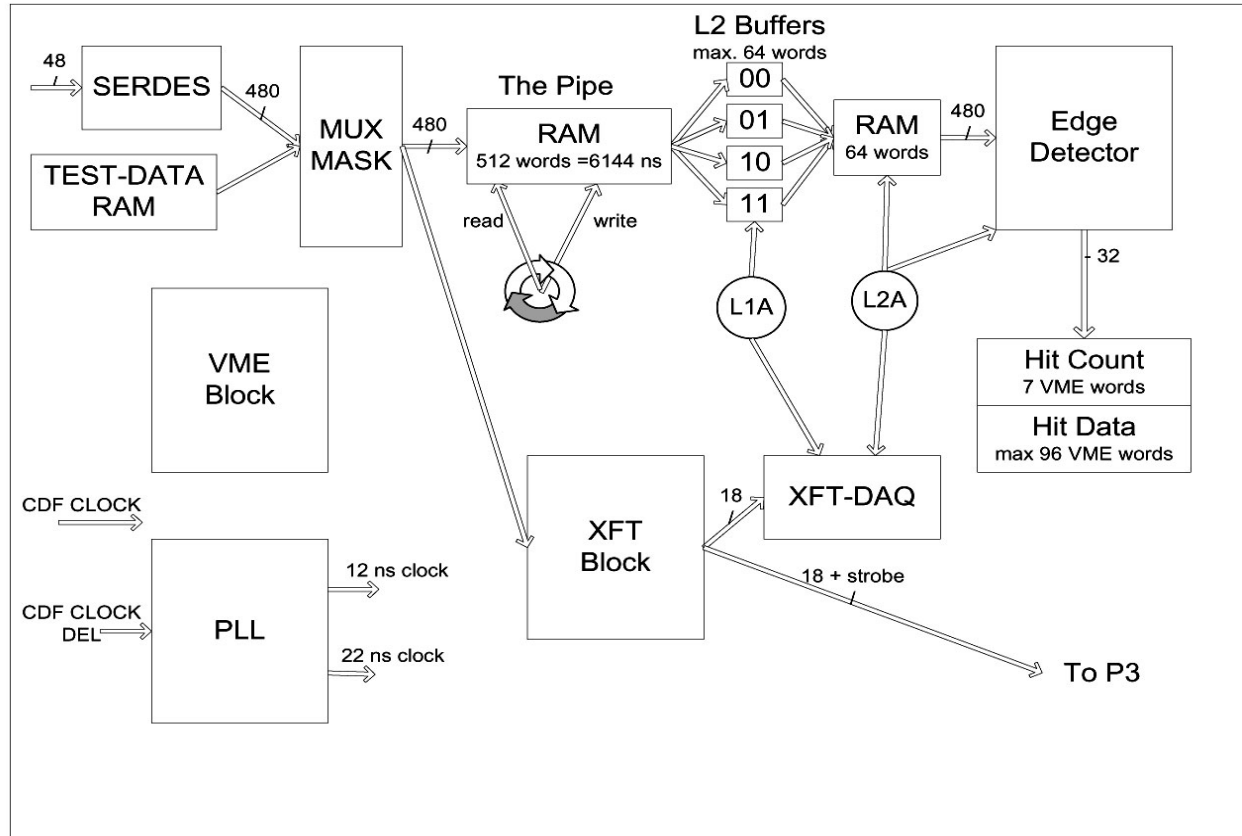
TIME-TO-DIGITAL



TIME-TO-DIGITAL CONVERSION: 1.2ns sampling rate

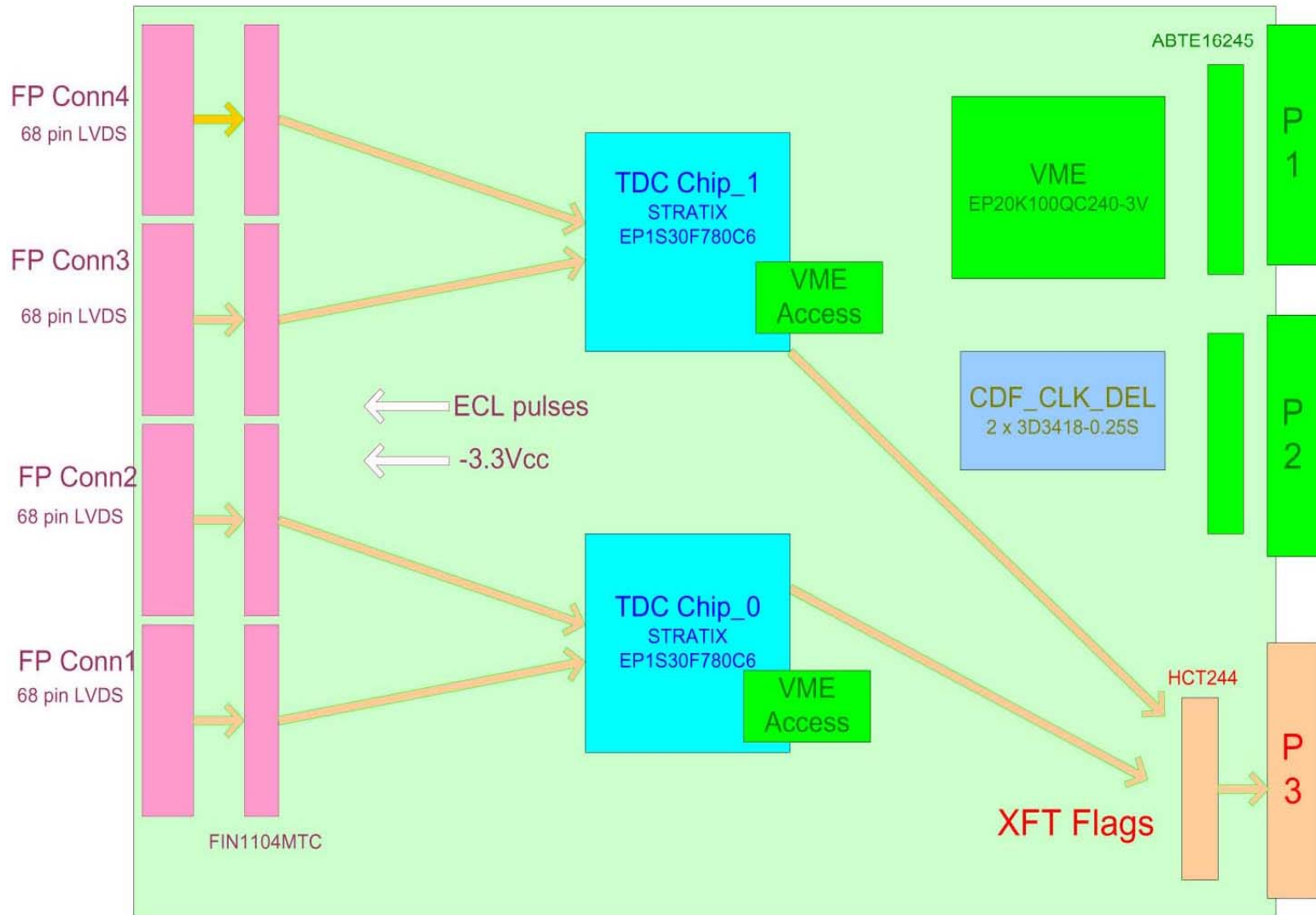
`serdes_in` ~ 20 ns LVDS pulse in the simulation window of QuartusII

TDC Chip – Data Flow



STRATIX-EP1S30F780C6- Block Diagram

TDC Board– Data Flow



TDC Board– Specifications

- For P0,P1,P2 and Front-panel, the board has the same connections as The Old TDC;
- 96 LVDS inputs – same termination scheme as The Old TDC;
- Pipe-Line Size: 512 words(6,144 us);
- Test Data RAM Size: same as the Pipe-Line;
- L2 Buffers length – max 64 words(768ns), simulated for 34 words;
- L2 Buffers are not VME accessible but have a known power-up value for testing;
- Accepts successive L1A pulses on 132ns intervals;
- On the next CDF Clock after L2A, the L2 Buffer is available for writing;
- Edge detection: 1 hit = min 4 “1” followed by min 4 “0”; records max 4 hits/wire;
- The results are ready for VME read-out ~7.25 us after a L2A.
- Min time interval between L2A pulses: ~7.25 us.
- Hit-Count Result: $4 \text{ bits/wire} \times 48 \text{ wires/chip} + 1 \text{ header word} = 7 \text{ VME words/chip}$;
- Hit-Data Result(max): $16 \text{ bits/hit} \times 4 \text{ hits/wire} \times 48 \text{ wires/chip} = 96 \text{ VME words/chip}$;

XFT

There are two modes of operation for the XFT Block

New Style:

- There are 6 continuous, non-overlapping time windows programmable in units of 12ns.
- The hit detection procedure: locate 4 sequential high cells in the input data stream (4.8ns).

Old Style:

- The same: PROMPT, NOTSURE and LATE windows from the old design and the resulting P3 output data follow the same truth table.

Old Design

- CDF_CLK is delayed with ~70ns in steps of 1ns, to bring it in sync with the crossing.
- Prompt/Delayed bits are sent out beginning with the NEXT, delayed(70ns)CDF_CLK.

New Design

- CDF_CLK is delayed with 0 to 12 ns in steps of 0.25 ns, using delay lines outside the chip.
- Data out P3 beginning with the SECOND delayed(with 0-12ns) CDF_CLK.

XFT DAQ

The XFT outputs are also routed to a buffer system, similar to the main one.

- We have a Pipe-Line, 4 L2 Buffers and a VME read-out buffer, all with the same number of words as the main DAQ.

- Differences:

- buffer width (18 bits) and write clock (22ns);

- this VME read-out buffer is not available for CBLT;

- Pipe Size and L2 Buffer Length are adjustable independently from the main DAQ;

One can corroborate the Hit-Count/Data results with information from the XFT DAQ.

For testing, the chips have also a XFT-OUT-RAM, that has the XFT flags.

TDC- Design Choices

- Parts:**
- factors considered: price, functionality;
 - FPGA for VME: EP20K100QC240-3V- \$45.
new design, includes CBLT, used ~15% of the logic elements.
 - FPGAs for the TDC Chips: 2 x EP1S30F780C6- \$465/pc.
uses +3.3V for I/O, +1.5V for internal cells,
can handle 48 – 840 MHz LVDS inputs, used ~65% of the logic elements,
not +5V tolerant => second set of buffers for the VME connections.
 - configuration devices: 2 x EPC16QC100 - \$55/pc and EPC2LC20 - \$21.

- Power:**
- limited by the number of power pins on backplane;
 - uses +5V/ 10A (estimated) and -5V/ 0.5A.
 - generates: +2.5V/3A Max with LM1085IT-Adj.;
 - generates: +3.3V/15A Max with DATEL UNR-3.3/15-D5 DC/DC;
will include the option to replace this with a linear regulator.
 - generates: +1.5V/20A/TDC Chip Max with DATEL UNR-1.5/20-D5 DC/DC;
we may use only one DC/DC converter for both TDC Chips.
 - generates: -3.3V/1.5A Max with UWR-3.3/4250-D5A DC/DC;

TDC- Design Choices

Configuration Options:

- Each FPGA has it's own JTAG Chain with a 10-pin connector inside the board;
- We can switch to one big chain with the two STRATIX Chips, two EPC16 and a 10-pin front panel connector.

Will include:

- Initiate STRATIX Chips device reconfiguration with one VME write command;
- Initiate VME Chip device reconfiguration with a pulse on P1/SYSRESET*;

Clock Distribution:

- CDF Clock from P2 to each STRATIX Chip used to latch L1A, L2A, B0, etc.
- CDF Clock from P2 is also applied to two programmable delay lines 3D3418-0.25S, by DDD. The max delay is 83ns in steps of 0.25ns. The delayed CDF Clock becomes reference for the TDC Chips' internal PLLs.
- Each FPGA is connected to on board Crystal Oscillators for testing.

CBLT

The TDC Board permits CBLT transactions as per ANSI/VITA 23-1998.

Two different CBLTs:

- From Slot 30, Addr YY900000 – Hit-Count Buffers – 14 words/board;
- From Slot 31, Addr YY800000 – Hit-Data Buffers – max 192 words/board;

Discrepancy between our VME crates and CBLT standard: will modify (kludge):

- Cut one trace on the backplane;
- Cut two traces and add two jumpers on the 6U/9U Extender Card.

Solution not compatible with an other possible slave in the crate that uses interrupts.

No need for a board to be designated as “First”.

Any board can be eliminated from the chain.

Design tested with 3 TDC boards in crate using default data in L2 Buffers (See Sasha).

In the test-crate at UC, measured approx. 200ns between successive `_DTACK` pulses, using MVME2301 with default timing settings.

Board Specifications

MGC File Geometries Setup Check Report View Help Support

DR\$Specification V A I O R

Selected: 0 Line Width: 0.0
 Delta: 16.2, -3.4 Abs: 16.2, -3.4 In. Grid: X 0.05, DRAWING 1

Comp.Side

Layer Order	Material
1.Signal_1	Microstrip
2.Player_0R	
3.Signal_2	Stripline
4.Player_0R	
5.Signal_3	
6.Player_+1.5R	
7.Player_-0.5R -3.2R	
8.Signal_4	
9.Player_+2.5R	
10.Signal_5	
11.Player_+3.2R	
12.Signal_6	

Board Characteristics

- All dimensions are given in inches unless specified otherwise.
- Material FR4 with $\rho > 1700$. E.g. FR402.
- Minimum trace width and clearance: 0.008" on Signal 1,6 (Top and Bottom).
- Minimum trace width and clearance: 0.008" on Signal 2,3,4,8 (all stripline traces).
- 1/2 oz copper for all copper layers and for Signal 1,3 (Top and Bottom).
- 1/2 oz copper for Stripline trace layers (Signal 2,3,4,8).
- Impregnation Gold over copper, with min. Ni: 2.5-5 μ m; Au: 0.05-0.2 μ m.
- Apply solder mask over bare copper.
- Spacing in through holes: 0.008" +/- 0.003
- Mill the top and bottom of boards on the solder side to a thickness of 0.002" +/- 0.000
- 35 degrees on Component and Solder Sides.
- 45 degree elsewhere.
- Fit tolerances +/- 0.002 unless specified otherwise.
- Inter layer spacing as specified.
- Top is a prepreg'd prepreg, thru hole with the following specs:
 - 12-1. Finished plated hole size: 0.05 - 0.05 mm.
 - 12-2. Drilled hole size: 0.2mm +/- 0.002mm.
 - 12-3. Min. thickness of thru hole plating: Cu: 25 μ m; Ni: 2.5-5 μ m; Au: 0.05-0.2 μ m.
- 20-50 Dwg +/- B Dwg for 0.008" stripline and 0.008" microstrip traces on all layers. Perform TDP test for all signal layers, using coating test traces on board. Report TDP test results for all signal layers.

BOARD'S DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
O	.014	1550	YES	----	
B	.018	2398	YES	----	
B	.05	350	YES	----	
B	.0285	837	YES	----	Note 12., Note 12.
B	.085	777	YES	----	
B	.041	776	YES	----	
B	.047	60	YES	----	
D	.06	1	YES	----	
B	.092	20	YES	----	
B	.097	49	YES	----	
B	.098	12	YES	----	
B	.106	9	NO	----	
B	.113	6	NO	----	
B	.12	8	YES	----	
B	.16	2	YES	----	

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TDC Board
Specification Drawing

DATE: 1/4

```

$$$close_window(@discard);
$set_active_window("BO$9UVME");
$$$draw_parts("Specification");
    
```

TDC- Layout Top

MGC File Geometries Setup Check Report Properties View Help Support

BO\$9UVME V A I O R

Selected: 0 Check On Components: 930 (0) Line Width: 0.0
Delta: 4.97035, -2.3069 Abs: 2.0, -18.35 In. Grid: X 0.05, DRAWING 1

BOARD: Top

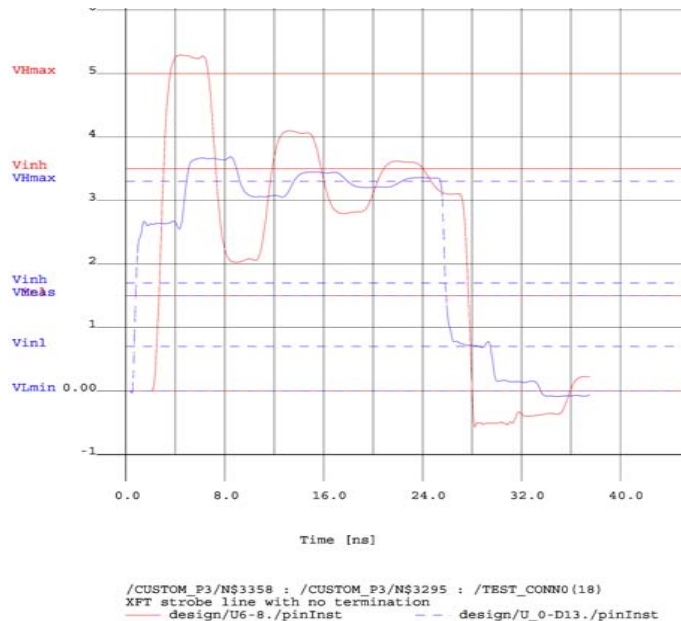
SESSION ? HELP ?
SHAPES TEXT
DRILL MILL
AREA FILL CHANGE REF
ART WORK BOARD

```
$view_layers(["SIGNAL_2", "SIGNAL_3", "SIGNAL_4", "SIGNAL_5", "SIGNAL_6"],@remove  
$view_layers(["PIN_ID_2", "SILKSCREEN_1", "SILKSCREEN_2", "SHEET_DIELECTRIC_3", "  
I_2"],@remove);
```

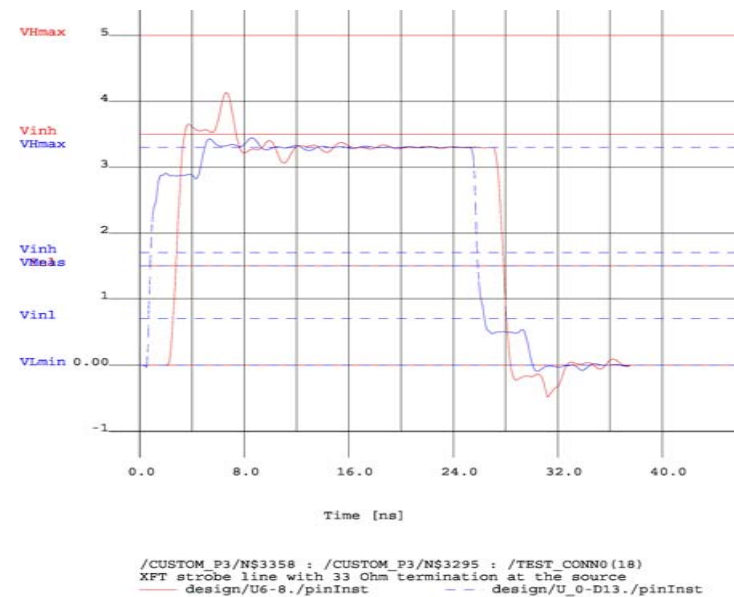
Trace Analysis and Functional Simulation

We performed signal integrity test on some nets on the board using the ICX tool by MGC. Most of the IBIS models are vendor supplied.

With NO Termination.



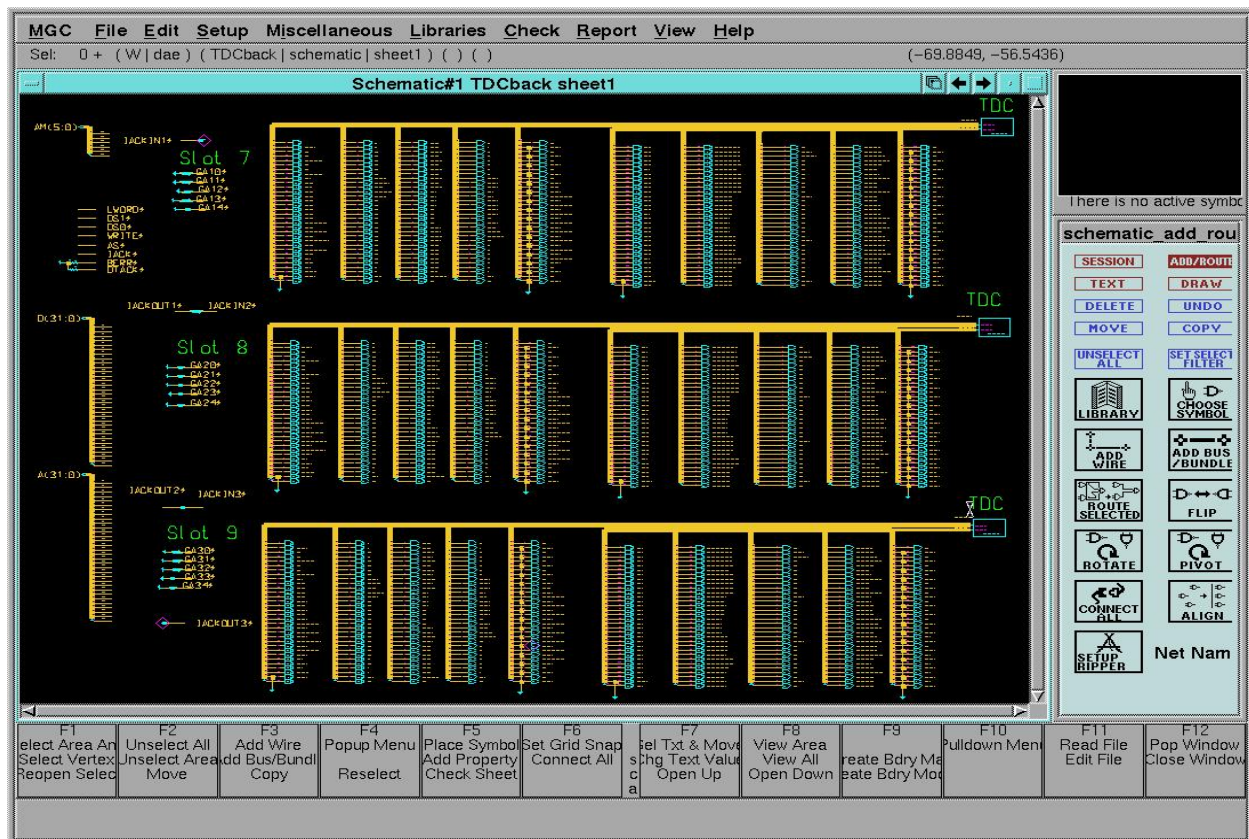
With 330hm Series Termination on the Source.



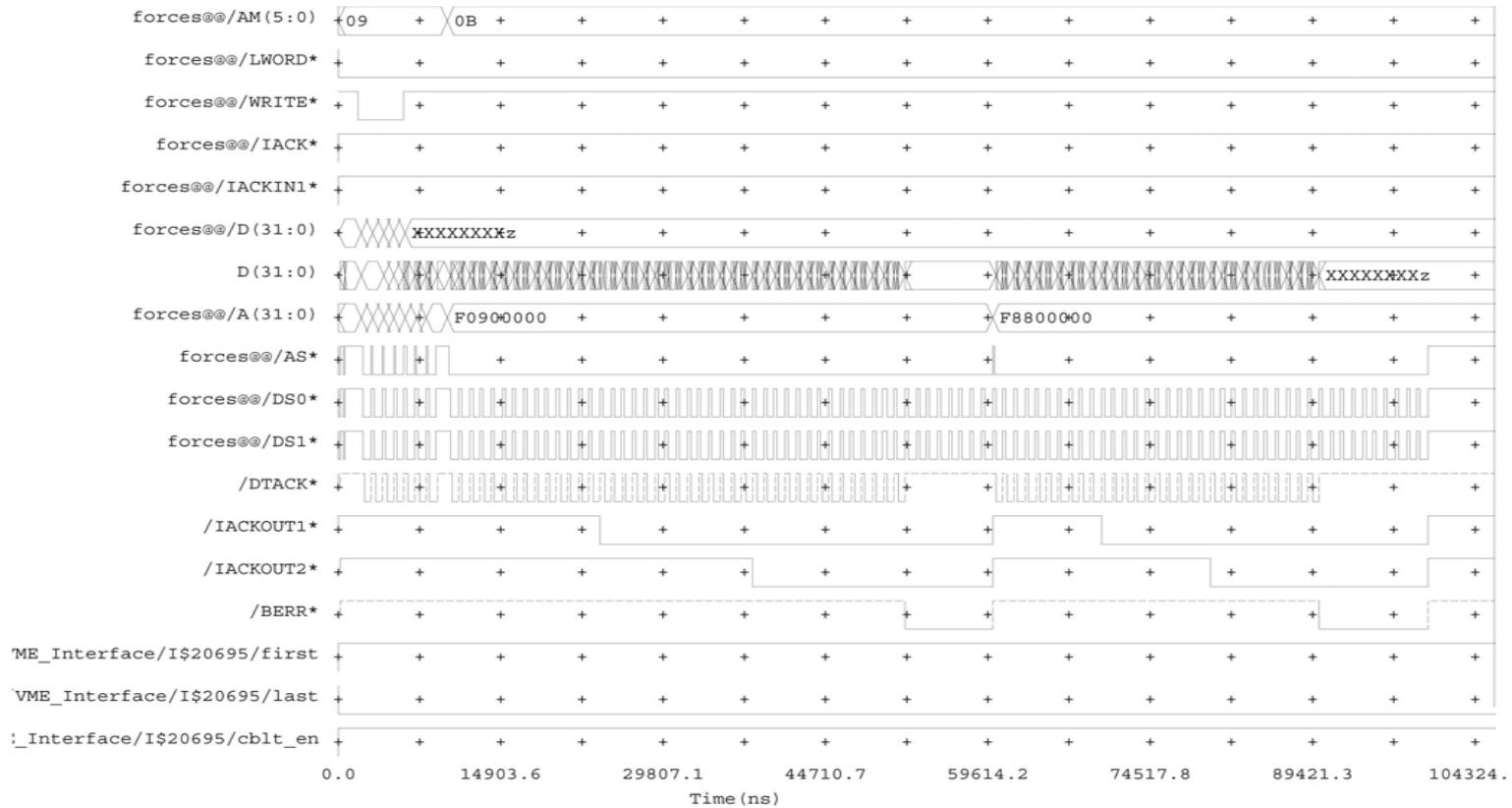
Functional Simulation: Each FPGA was first simulated with QuartusII 3.0. Files imported in QSII ; only the VME transactions were simulated with QSII.

Multi-Board simulation

Instantiated 3 TDC boards in a top level schematic with DA to simulate a CBLT transaction



Multi-Board Simulation



CBLT transaction simulated with QuickSimII by MGC.

Signal Tap-CBLT

CBLT transactions were observed using SignalTap™ embedded logic analyzer.

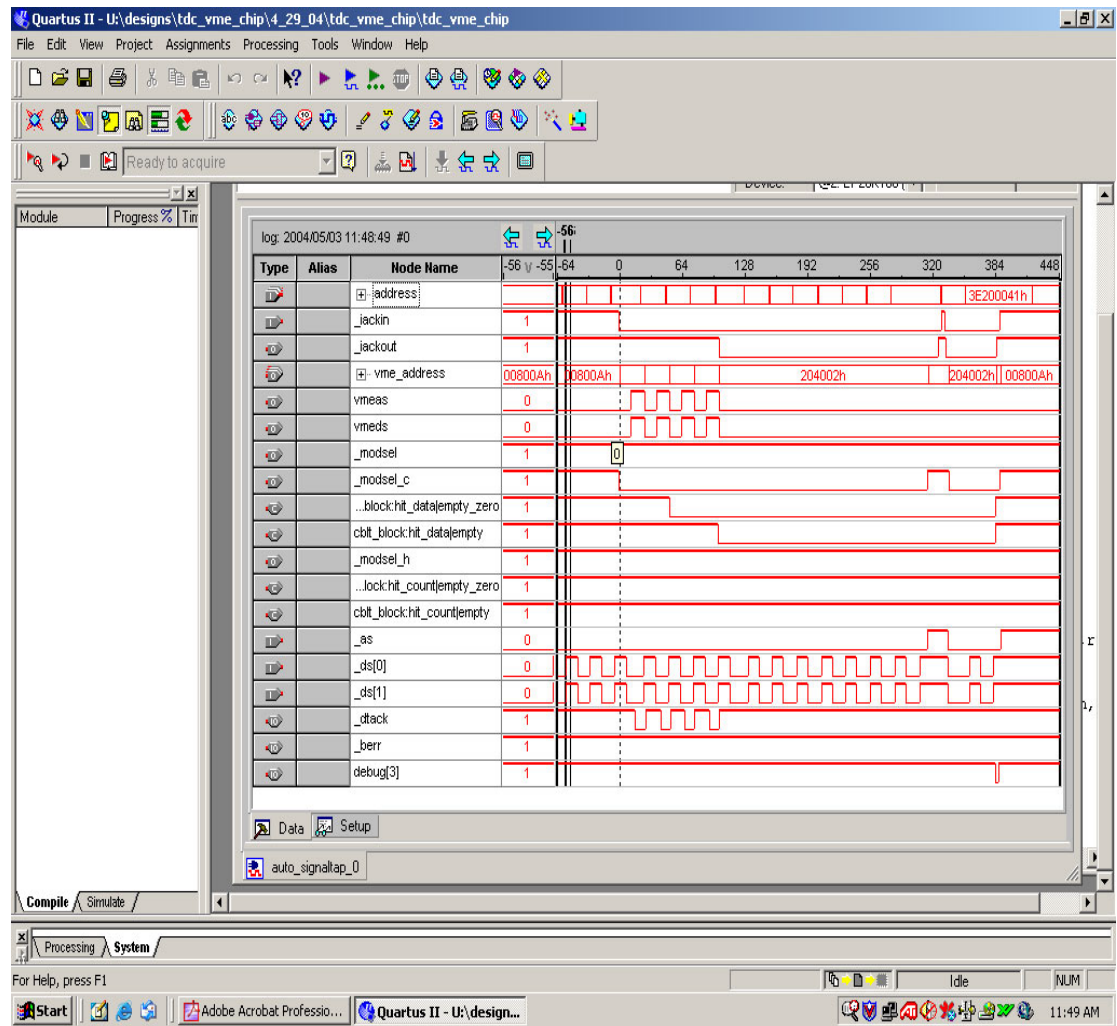
Here, the function was compiled into the VME Chip of the 2nd board.

We read $52+4+10 = 66$ words from the 3 TDC boards in the crate.

Logic analyzer:

- 512 samples;
- 50/100 MHz sampling clock;
- Trigger on `_IACKIN`.

SignalTap™ proved very beneficial for debugging the firmware and checking performance.



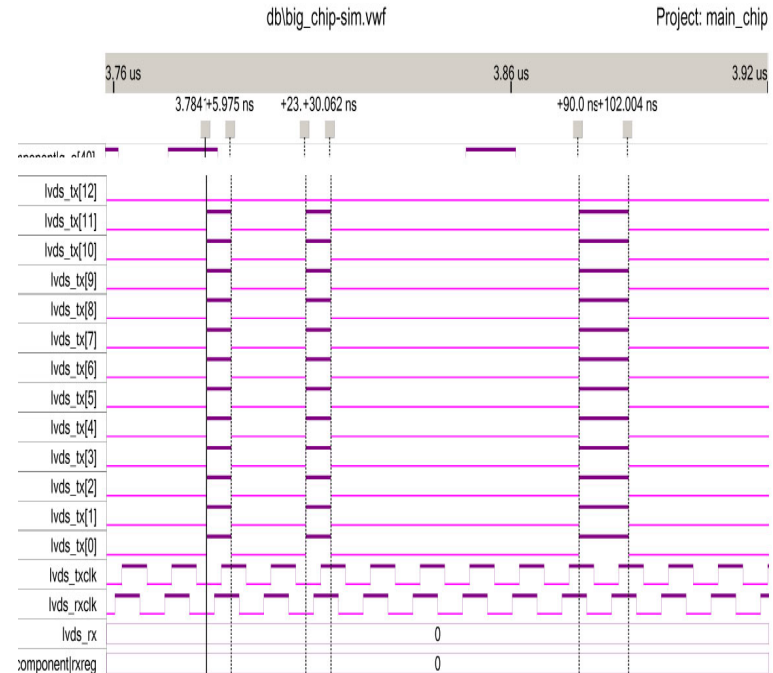
Pulse testing

Implemented a 12 channel, LVDS test pattern generator with our STRATIX development board, that can be plugged in any of the 4 front panel connectors of the TDC.

In this example, the pattern is the same on each wire pair and repeats every 396ns, not in phase with the CDF clock.

For the other 12 input pairs on the connector, the negative input is connected to GND to avoid crosstalk.

Generated L1A with the TestClock and L2A via VME and examined the hit-count and hit-data info from the VME read-out buffers.



To Do List

Modifications required for preproduction:

1. Add one new line from P1/C11-BERR* to the VME chip through an existing buffer for the CBLT event completion, as per ANSI/VITA23-1998, Observation E.7-c.

Added features:

1. Include a mux & buffer circuitry to allow Front Panel ECL Calibration Pulse origin change from the backplane to the on-board Stratix Chip_0. The selection is made via VME. This local 12 ns pulse comes after each B0 with a VME controlled delay.

2. Add two extra lines on the PCB to initiate reconfiguration of both Stratix chips with one VME write operation.

3. Add one more line from the backplane (P1/C12-SYSRESET*) to initiate reconfiguration of the VME chip (all boards in crate).

4. Include 2 test-points to allow connection of the outputs of the two +1.5V power supplies and then not stuff one of them. This will save some \$100/board.

5. Design an other +3.3V power supply, a linear one, place it next to the old one and not stuff the old one. This, again, will save some \$100/board.

6. Provide front panel LEDs for the -5V and, -3.3V power supplies.

7. Provide a front-panel resettable circuit breaker (the same component as for the old TDC), for the -3.3V power supply.

Conclusions

The four prototypes work as designed (one blue wire).
All the changes are already implemented in the TDC Schematic.
The artwork changes can be finalized in one week.