TDC Testing Status

1. Edge Detector test for up to 7 hits per channel:

The boards seem to work fine, some problems:

- Last compilation has few timing warnings(XFT Block), unsure if is causes problems of not… have to fix that…
- Sometimes… odd configuration problems …changed JTAG Chain from 4 devices to 2x2 devices on one board …have to look into that…
- Some problems with the Test-clock/Backplane: no L1A at some buffers…

2. CBLT32/64 transfers tested, using MVME2301(scope plots):
   - 416 Bytes(CBLT32) - 22.83 us on *AS line => 18.22 MB/s;
   - 416 Bytes(CBLT64) - 11.60 us on *AS line => 35.86 MB/s.

To do:
- Repeat the test with new Crate CPU?
- Finish CBLT64 firmware (same number of Bytes for 32/64, etc.,…)
- Write and perform CBLT64 multi-million, automated test (Sasha).

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3. LVDS Pulse tests using Altera Dev. Board as Test Pattern Generator.

   The "edge-detected" pulse widths and time intervals between pulses seem to be fine. See transcript (uncommented).

4. XFT Tests: new firmware seems to work fine (see Sasha).

Prepared Board 4 and Board 5 for testing at Fermilab.