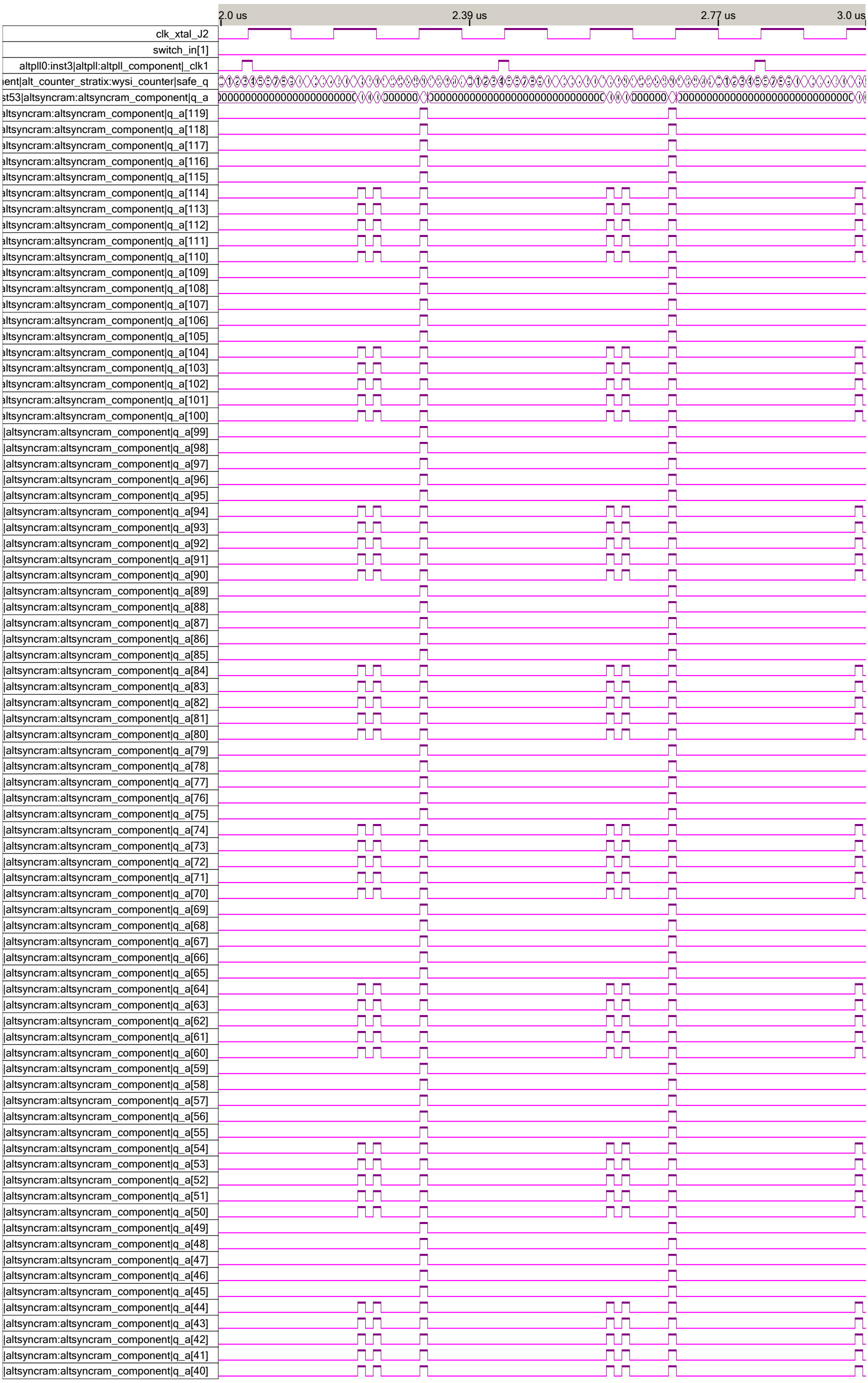
2.0 us
2.39 us
2.77 us
3.0 us
clk_xtal_J2
switch_in[1]
altpll0:inst3|altpll:altpll_component|_clk1
ent|alt_counter_stratix:wysi_counter|safe_q
st53|altsyncram:altsyncram_component|q_a
altsyncram:altsyncram_component|q_a[119]
altsyncram:altsyncram_component|q_a[118]
altsyncram:altsyncram_component|q_a[117]
altsyncram:altsyncram_component|q_a[116]
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|altsyncram:altsyncram_component|q_a[41]
|altsyncram:altsyncram_component|q_a[40]

2.0 us
2.39 us
2.77 us
3.0 us
|altsyncram:altsyncram_component|q_a[39]
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lvds_tx[1]
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lvds_txclk
lvds_rxclk
lvds_rx
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altpll0:inst3|altpll:altpll_component|_clk0
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ioport_one[17]
switch_in[14]
switch_in[15]
ent|alt_counter_stratix:wysi_counter|safe_q
ioport_one[0]
ioport_one[1]
ioport_one[2]
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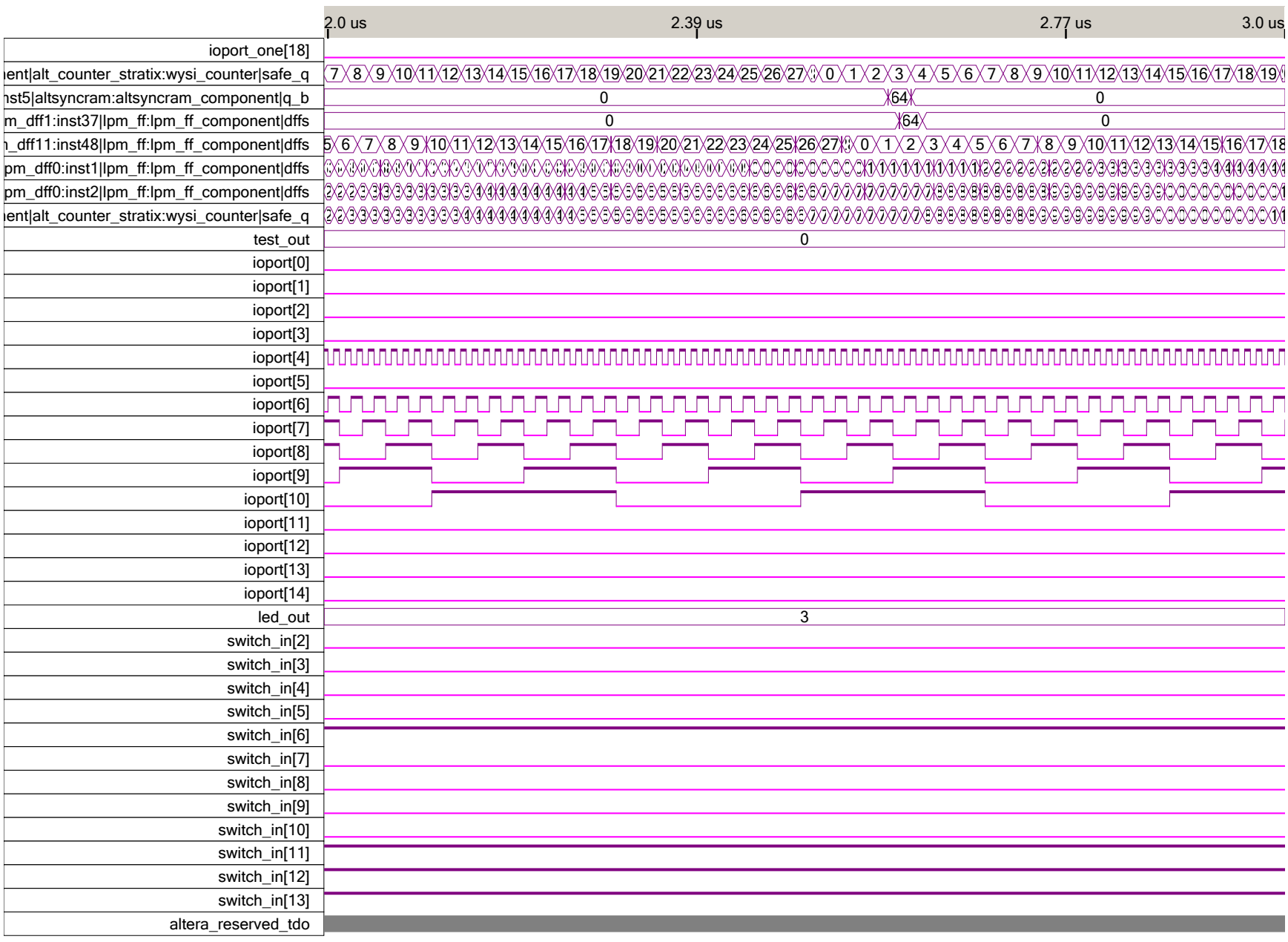
ioport_one[15]
ioport_one[16]


2.0 us
2.39 us
2.77 us
3.0 us
ioport_one[18]
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nst5|altsyncram:altsyncram_component|q_b
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_dff11:inst48|lpm_ff:lpm_ff_component|dffs
pm_dff0:inst1|lpm_ff:lpm_ff_component|dffs
pm_dff0:inst2|lpm_ff:lpm_ff_component|dffs
ent|alt_counter_stratix:wysi_counter|safe_q
test_out
ioport[0]
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ioport[2]
ioport[3]
ioport[4]
ioport[5]
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ioport[14]
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switch_in[12]
switch_in[13]
altera_reserved_tdo