

B2714 BOARD SPECIFICATIONS

1. Board Layers: 8
2. Layer Stack Order:

Layer1 (Artwork_1): Top component layer (Signal_1), 0.5oz, Z(diff)=100 ohm
 Layer2 (Artwork_2): Power_1 (GROUND), 1oz
 Layer3 (Artwork_3): Power_2/Power_3/Power_4 (VCCA2V5/VCCHGXB2V5/VCCLGXB1V2), 1oz
 Layer4 (Artwork_4): Inner SIGNAL_3, 0.5 oz, Z(single_end)= 50 ohm
 Layer5 (Artwork_5): Power_5/Power_6 (VCCINT1V2/VCCDLL1V2), 1oz
 Layer6 (Artwork_6): Inner SIGNAL_4, 0.5 oz, Z(single_end)= 50 ohm
 Layer7 (Artwork_7): Power_7/Power_8/Power_9 (P3V3/P2V5/P1V2), 1oz
 Layer8 (Artwork_8): Bottom component layer (signal_2), 0.5oz, Z(diff)=100 ohm

3. Apply silkscreen on both side:

Artwork_9: Top silkscreen.
 Artwork_10: Bottom silkscreen

4. Apply solder mask over bare copper on both side:

Artwork_11: Top solder mask
 Artwork_12: Bottom solder mask

5. Material: FR4

6. Board thickness: 0.062" +/- 0.010.

7. Send me layer thickness specification for impedance verification

8. Copper thickness 1oz before plating for all the power planes.

9. Copper thickness 0.5oz before plating for all the signal layers.

10. Immersion Ni/Au finish over bare copper

11. Differential pairs: trace/gap/trace=5/5/5 mils

12. All differential pairs impedance Z(diff) controlled at 100 ohm (+/-10%)

13. All other traces minimum clearance = 5 mils

14. All dimensions are in inches unless otherwise noted.

Contact person:

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SCH# B2713

SPC# B2714

ASM# B2715

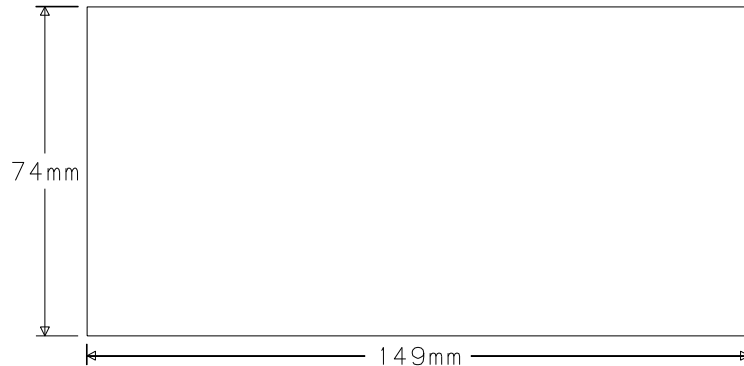
UNIVERSITY OF CHICAGO
 ELECTRONICS DEVELOPMENT GROUP

TITLE

B2714 specifications

SHEET 1 OF 1
 DATE 03/22/2011
 DRAWN TANG

B-2714
 REV 1.0



BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.01	650	YES	---
⊞	.015	70	YES	---
⊘	.02	23	YES	---
⊞	.035	2	YES	---
⊘	.037	18	YES	---
⊞	.041	56	YES	---
⊘	.055	2	YES	---
□	.062	4	YES	---
	.10629921	5	YES	---