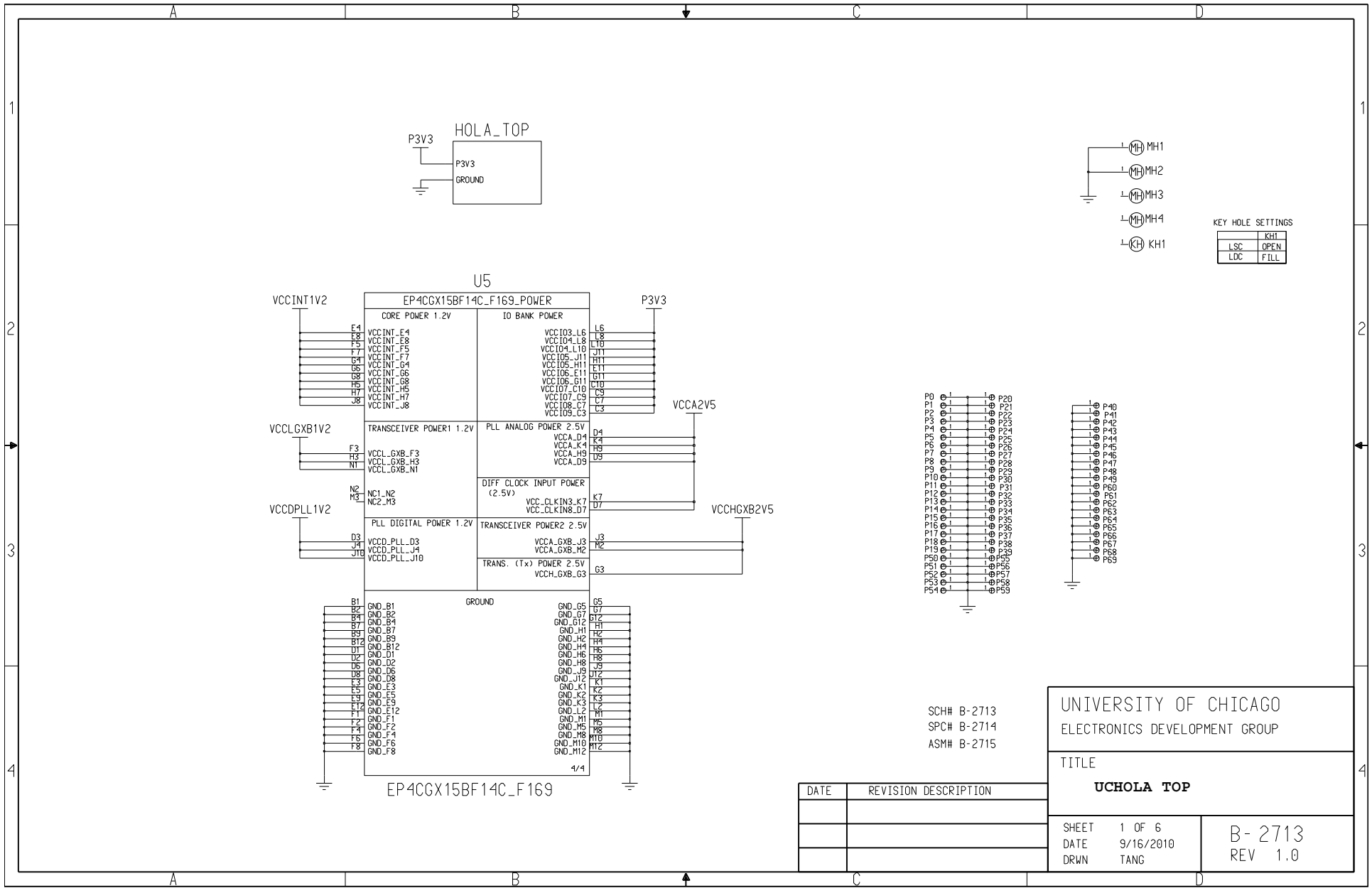
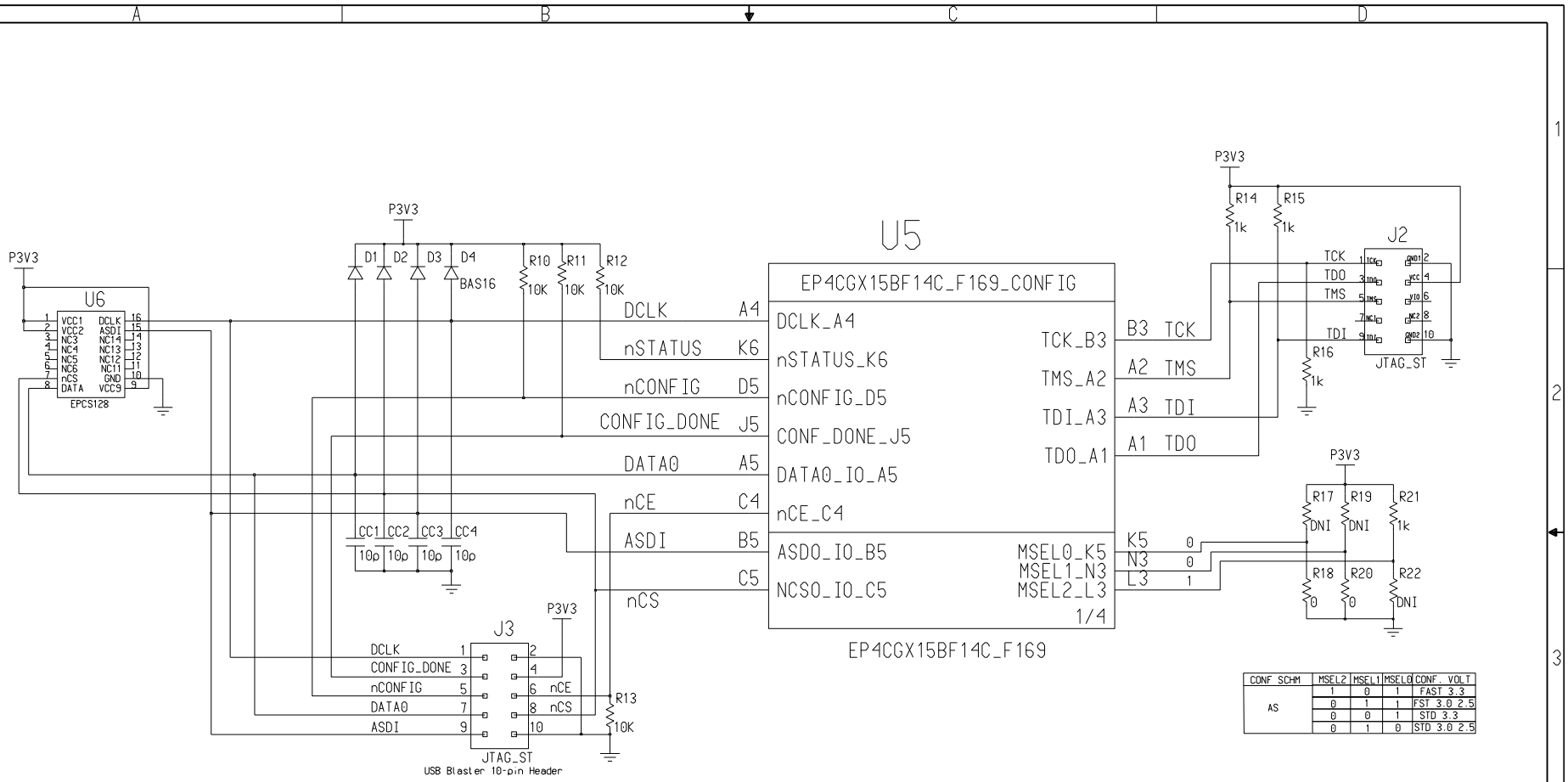
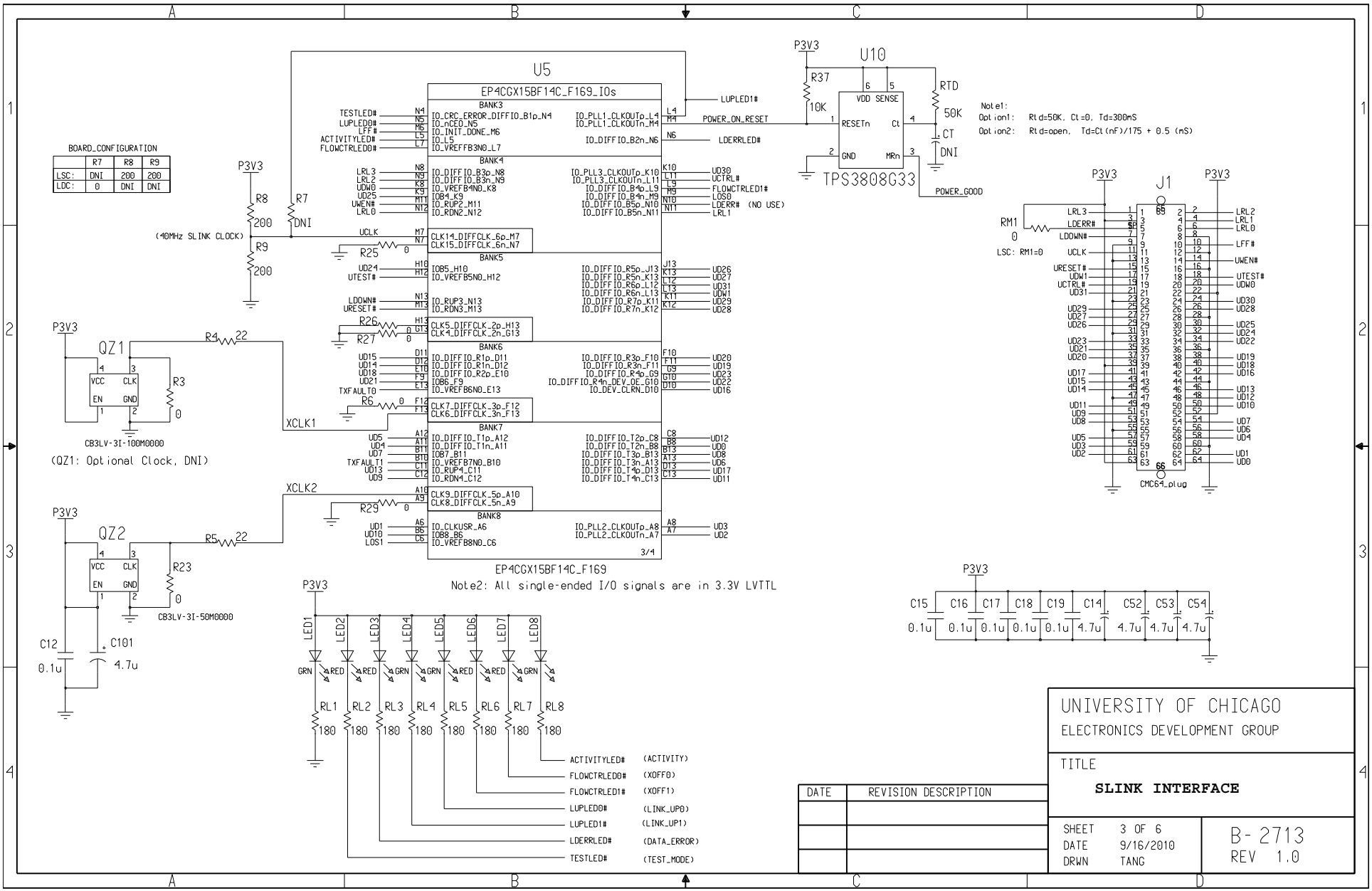
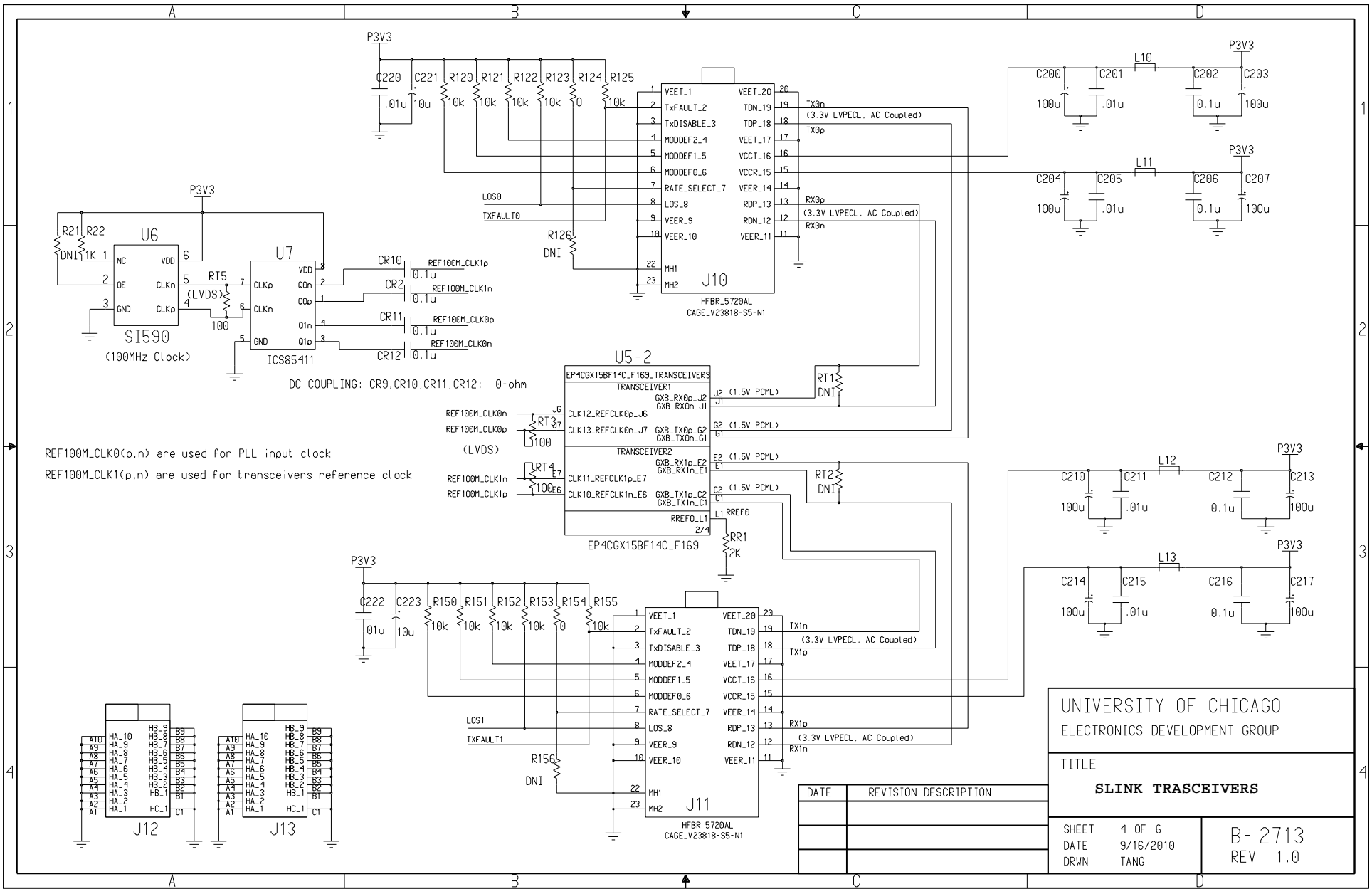
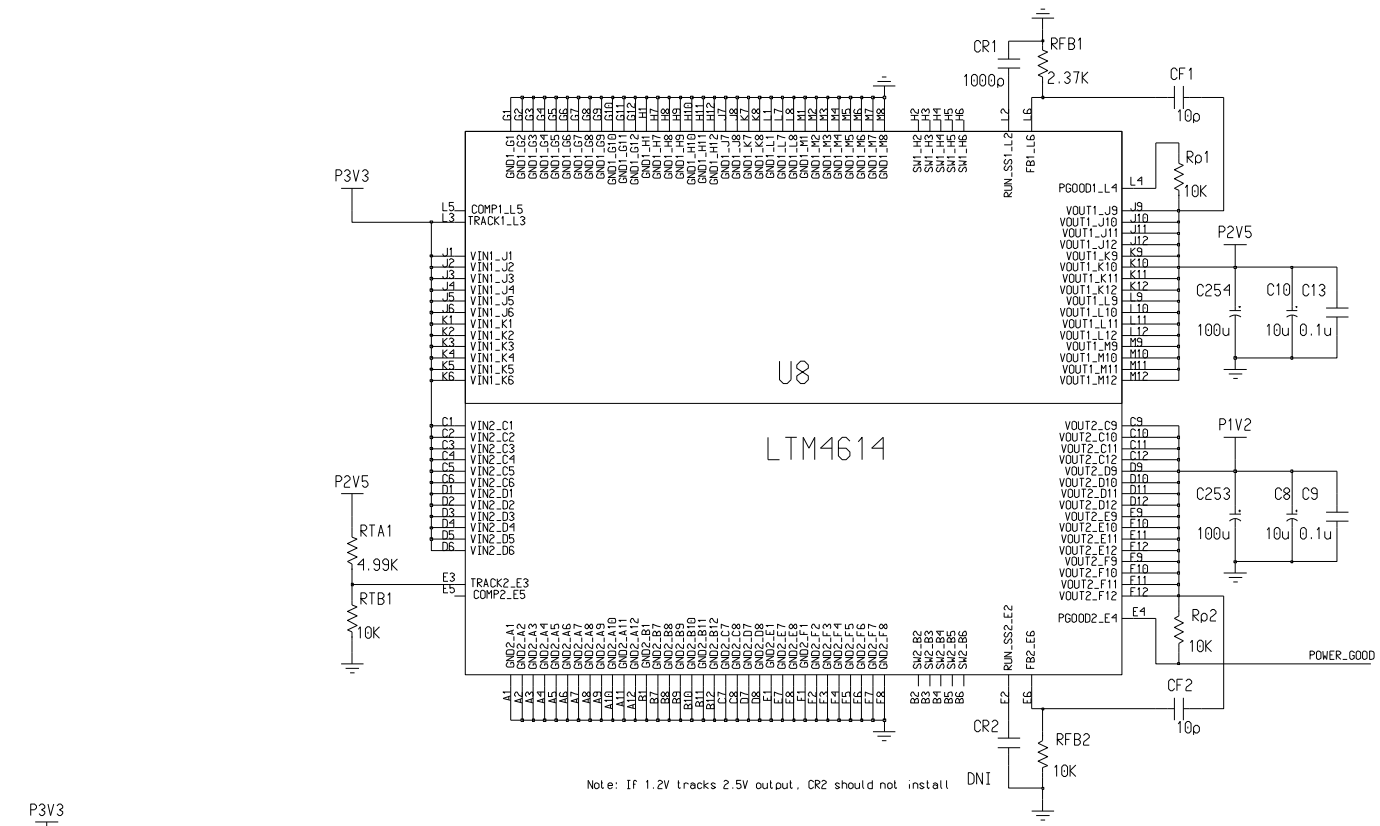
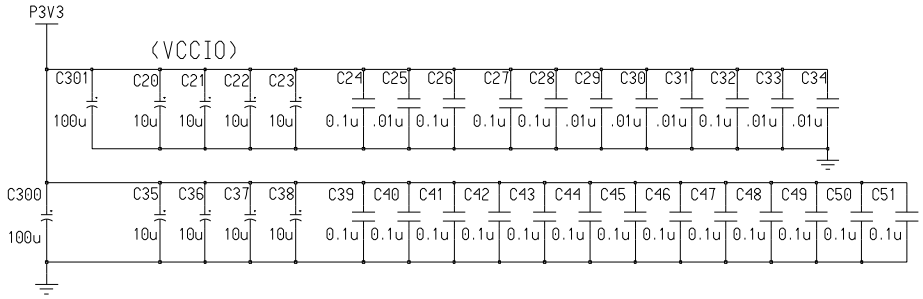

HOLA_TOP
P3V3
P3V3
GROUND
MH1
MH2
MH3
MH4
KH1
KEY HOLE SETTINGS
KH1
LSC OPEN
LDC FILL
U5
EP4CGX15BF14C_F169_POWER
CORE POWER 1.2V
IO BANK POWER
TRANSCEIVER POWER1 1.2V
PLL ANALOG POWER 2.5V
DIFF CLOCK INPUT POWER (2.5V)
PLL DIGITAL POWER 1.2V
TRANSCEIVER POWER2 2.5V
TRANS. (Tx) POWER 2.5V
GROUND
VCCINT1V2
VCCLGXB1V2
VCCDPLL1V2
VCCA2V5
VCCHGXB2V5
P3V3
VCCINT_E4
VCCINT_E8
VCCINT_F5
VCCINT_F7
VCCINT_G4
VCCINT_G6
VCCINT_G8
VCCINT_H5
VCCINT_H7
VCCINT_J8
VCCIO3_L6
VCCIO4_L8
VCCIO4_L10
VCCIO5_J11
VCCIO5_H11
VCCIO6_E11
VCCIO6_G11
VCCIO7_C10
VCCIO7_C9
VCCIO8_C7
VCCIO9_C3
VCCL_GXB_F3
VCCL_GXB_H3
VCCL_GXB_N1
VCCA_D4
VCCA_K4
VCCA_H9
VCCA_D9
NC1_N2
NC2_M3
VCC_CLKIN3_K7
VCC_CLKIN8_D7
VCCD_PLL_D3
VCCD_PLL_J4
VCCD_PLL_J10
VCCA_GXB_J3
VCCA_GXB_M2
VCCH_GXB_G3
GND_B1
GND_B2
GND_B4
GND_B7
GND_B9
GND_B12
GND_D1
GND_D2
GND_D6
GND_D8
GND_E3
GND_E5
GND_E9
GND_E12
GND_F1
GND_F2
GND_F4
GND_F6
GND_F8
GND_G5
GND_G7
GND_G12
GND_H1
GND_H2
GND_H4
GND_H6
GND_H8
GND_J9
GND_J12
GND_K1
GND_K2
GND_K3
GND_L2
GND_M1
GND_M5
GND_M8
GND_M10
GND_M12
4/4
EP4CGX15BF14C_F169
P0 P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15 P16 P17 P18 P19 P50 P51 P52 P53 P54
P20 P21 P22 P23 P24 P25 P26 P27 P28 P29 P30 P31 P32 P33 P34 P35 P36 P37 P38 P39 P55 P56 P57 P58 P59
P40 P41 P42 P43 P44 P45 P46 P47 P48 P49 P60 P61 P62 P63 P64 P65 P66 P67 P68 P69
SCH# B-2713
SPC# B-2714
ASM# B-2715
DATE
REVISION DESCRIPTION
UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP
TITLE
UCHOLA TOP
SHEET 1 OF 6
DATE 9/16/2010
DRWN TANG
B-2713
REV 1.0


U5
EP4CGX15BF14C_F169_CONFIG
DCLK_A4
nSTATUS_K6
nCONFIG_D5
CONF_DONE_J5
DATA0_IO_A5
nCE_C4
ASDO_IO_B5
NCSO_IO_C5
TCK_B3
TMS_A2
TDI_A3
TDO_A1
MSEL0_K5
MSEL1_N3
MSEL2_L3
1/4
EP4CGX15BF14C_F169
U6
EPCS128
J2
JTAG_ST
J3
JTAG_ST
USB Blaster 10-pin Header
P3V3
BAS16
DCLK
nSTATUS
nCONFIG
CONFIG_DONE
DATA0
nCE
ASDI
nCS
TCK
TDO
TMS
TDI
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
1k
10K
10p
DNI
CONF SCHM
MSEL2
MSEL1
MSEL0
CONF. VOLT
AS
FAST 3.3
FST 3.0 2.5
STD 3.3
STD 3.0 2.5
UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP
TITLE
IN-SYSTEM CONFIGURATION
DATE
REVISION DESCRIPTION
SHEET 2 OF 6
DATE 9/16/2010
DRWN TANG
B-2713
REV 1.0


U5
EP4CGX15BF14C_F169_IOs
EP4CGX15BF14C_F169
Note2: All single-ended I/O signals are in 3.3V LVTTL
U10
TPS3808G33
Note1:
Option1: Rtd=50K, Ct=0, Td=300mS
Option2: Rtd=open, Td=Ct(nF)/175 + 0.5 (mS)
J1
CM64_plug
BOARD_CONFIGURATION
R7 R8 R9
LSC: DNI 200 200
LDC: 0 DNI DNI
(40MHz SLINK CLOCK)
QZ1
QZ2
CB3LV-3I-100M0000
CB3LV-3I-50M0000
(QZ1: Optional Clock, DNI)
XCLK1
XCLK2
LED1 LED2 LED3 LED4 LED5 LED6 LED7 LED8
RL1 RL2 RL3 RL4 RL5 RL6 RL7 RL8
ACTIVITYLED# (ACTIVITY)
FLOWCTRLED0# (XOFF0)
FLOWCTRLED1# (XOFF1)
LUPLED0# (LINK_UP0)
LUPLED1# (LINK_UP1)
LDERRLED# (DATA_ERROR)
TESTLED# (TEST_MODE)
POWER_ON_RESET
POWER_GOOD
LUPLED1#
LDERRLED#
UCLK
UCTRL#
FLOWCTRLED1#
LOS0
LDERR# (NO USE)
LRL1
UWEN#
UTEST#
UDW0
UDW1
LFF#
TXFAULT0
TXFAULT1
UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP
TITLE
SLINK INTERFACE
SHEET 3 OF 6
DATE 9/16/2010
DRWN TANG
B-2713
REV 1.0
DATE
REVISION DESCRIPTION


P3V3
C220 .01u
C221 10u
R120 10k
R121 10k
R122 10k
R123 10k
R124 0
R125 10k
J10
HFBR_5720AL
CAGE_V23818-S5-N1
TX0n
(3.3V LPVECL, AC Coupled)
TX0p
RX0p
(3.3V LPVECL, AC Coupled)
RX0n
LOS0
TXFAULT0
R126 DNI
L10
L11
C200 100u
C201 .01u
C202 0.1u
C203 100u
C204 100u
C205 .01u
C206 0.1u
C207 100u
U6
SI590
(100MHz Clock)
R21 DNI
R22 1K
U7
ICS85411
RT5 100
(LVDS)
CR10 0.1u
CR2 0.1u
CR11 0.1u
CR12 0.1u
REF100M_CLK1p
REF100M_CLK1n
REF100M_CLK0p
REF100M_CLK0n
DC COUPLING: CR9,CR10,CR11,CR12: 0-ohm
U5-2
EP4CGX15BF14C_F169_TRANSCEIVERS
TRANSCEIVER1
TRANSCEIVER2
GXB_RX0p_J2
GXB_RX0n_J1
GXB_TX0p_G2
GXB_TX0n_G1
GXB_RX1p_E2
GXB_RX1n_E1
GXB_TX1p_C2
GXB_TX1n_C1
RREF0_L1
(1.5V PCML)
RT1 DNI
RT2 DNI
RT3 100
RT4 100
RR1 2K
EP4CGX15BF14C_F169
C210 100u
C211 .01u
C212 0.1u
C213 100u
C214 100u
C215 .01u
C216 0.1u
C217 100u
L12
L13
C222 01u
C223 10u
R150 10k
R151 10k
R152 10k
R153 10k
R154 0
R155 10k
J11
HFBR 5720AL
CAGE_V23818-S5-N1
TX1n
(3.3V LPVECL, AC Coupled)
TX1p
RX1p
(3.3V LPVECL, AC Coupled)
RX1n
LOS1
TXFAULT1
R156 DNI
J12
J13
REF100M_CLK0(p,n) are used for PLL input clock
REF100M_CLK1(p,n) are used for transceivers reference clock
UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP
TITLE
SLINK TRASCEIVERS
DATE
REVISION DESCRIPTION
SHEET 4 OF 6
DATE 9/16/2010
DRWN TANG
B-2713
REV 1.0





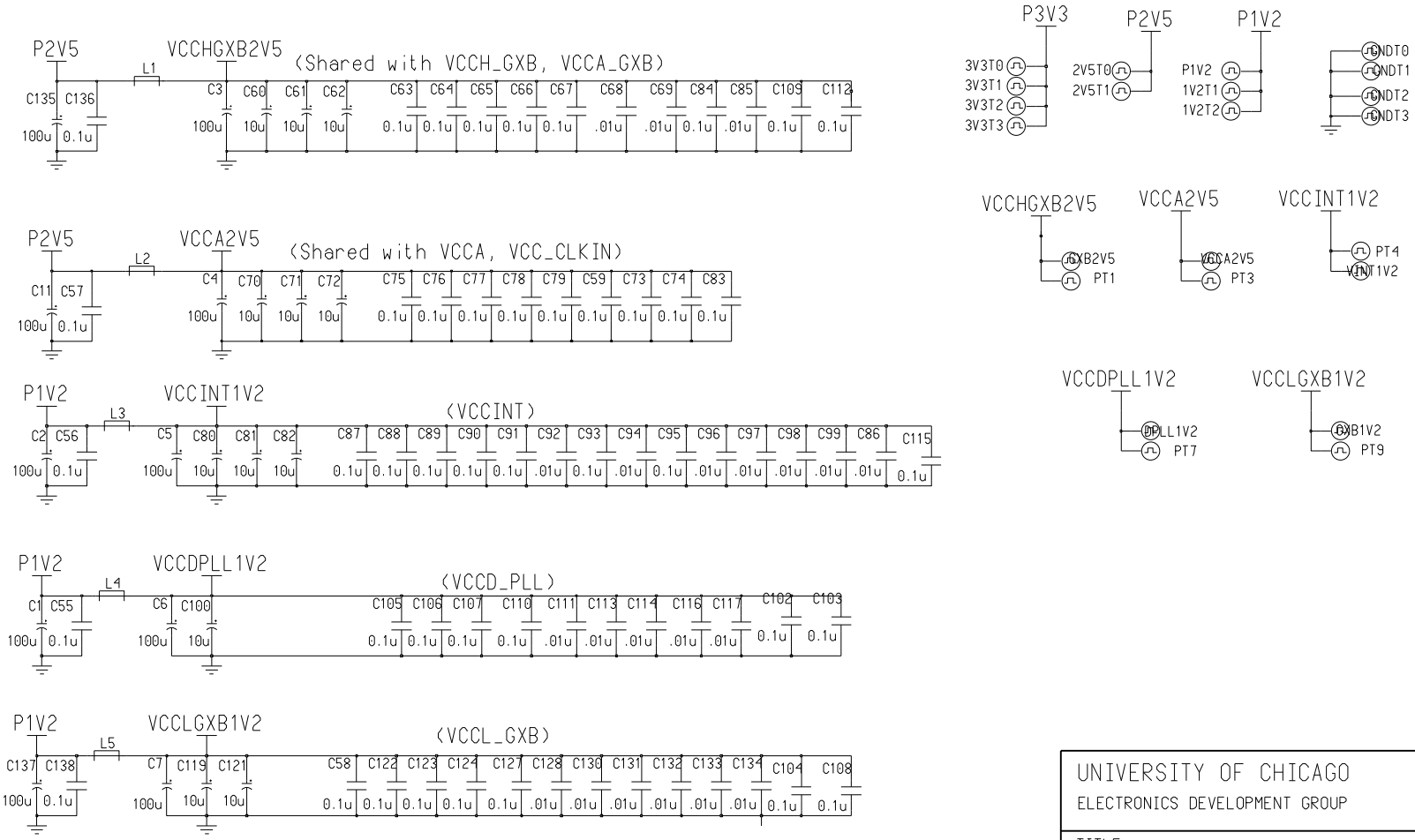
DATE	REVISION DESCRIPTION

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
LV POWER SUPPLIES

SHEET	5 OF 6
DATE	9/16/2010
DRWN	TANG

B-2713
REV 1.0



DATE	REVISION DESCRIPTION

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
LV POWER SUPPLIES (2)

SHEET 6 OF 6
DATE 9/16/2010
DRWN TANG

B-2713
REV 1.0

UCHOLA Board: Layer Stack-up

Fukun Tang (773)-834-4286

Artwork#	Physical Layer Name	Logical Signal Name	Plane Integrity	Routing Control	Note
Art1/L1	Top	Signal_1, Pad_1		Horizontal	(1)
Art2/L2	Power_1	GROUND	Full Plane		
ART3/L3	Power_2, Power_3, Power_4	VCCA2V5, VCCHGXB2V5, VCCLGXB1V2	Split Plane		
ART4/L4	Inner Signal_3	Signal_3		Horizotal	(2), (4)
ART5/L5	POWER_5, POWER_6	VCCINIT1V2, VCCDPLL1V2	Split Plane		
ART6/L6	Inner Signal_4	Signal_4		Horizontal	(2), (4)
ART7/L7	POWER_7, POWER_8, POWER_9	P3V3, P2V5, P1V2	Split Plane		
ART8/L8	Bottom	Signal_2, Pad_2		Vertical	(3), (4)

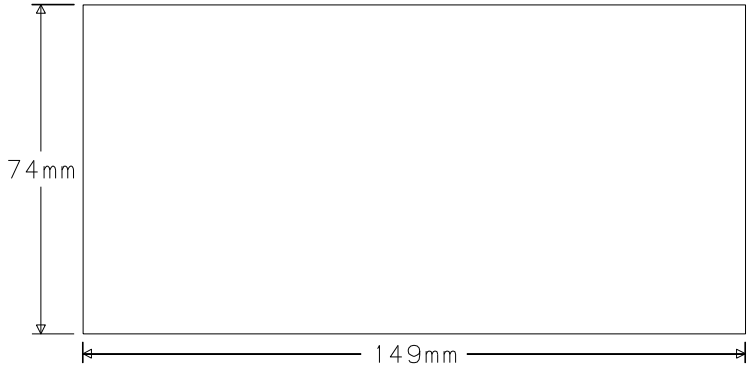
(1): No fast signal crosses the split gaps on the referenced power layers (for 2.5Gbps CML diff. signals)

(2): No fast signal crosses the split gaps on the referenced power layer (for 40Mbps TTL Signals)

(3): No fast signal crosses the split gaps on the referenced power layers (for 100MHz LVDS diff. signals)

(4): Filled with "ground" to help reduce inductance in signal return pathes and increase thermal conduct for uModule

B2514 BOARD SPECIFICATIONS



1. Board Layers: 8
2. Layer Stack Order:

Layer1 (Artwork_1): Top component layer (Signal_1), 0.5oz, Z(diff)=100 ohm
Layer2 (Artwork_2): Power_1 (GROUND), 1oz
Layer3 (Artwork_3): Power_2/Power_3/Power_4 (VCCA2V5/VCCHGXB2V5/VCCLGXB1V2), 1oz
Layer4 (Artwork_4): Inner SIGNAL_3, 0.5 oz, Z(single_end)= 50 ohm
Layer5 (Artwork_5): Power_5/Power_6 (VCCINT1V2/VCCDPLL1V2), 1oz
Layer6 (Artwork_6): Inner SIGNAL_4, 0.5 oz, Z(single_end)= 50 ohm
Layer7 (Artwork_7): Power_7/Power_8/Power_9 (P3V3/P2V5/P1V2), 1oz
Layer8 (Artwork_8): Bottom component layer (signal_2), 0.5oz, Z(diff)=100 ohm

3. Apply silkscreen on both side:
   Artwork_9: Top silkscreen.
   Artwork_10: Bottom silkscreen
4. Apply solder mask over bare copper on both side:
   Artwork_11: Top solder mask
   Artwork_12: Bottom solde mask
5. Material: FR4
6. Board thickness: 0.062'' +/- 0.010.
7. Send me layer thickness specification for impedance varification
8. Copper thickness 1oz before plating for all the power planes.
9. Copper thickness 0.5oz before plating for all the signal layers.
10. Immersion Ni/Au finish over bare copper
11. Differential pairs: trance/gap/trace=5/5/5 mils
12. All differential pairs impedance Z(diff) controlled at 100 ohm (+/-10%)
13. All other traces mininum clearance = 5 mils
14: All dimensions are in inches unless otherwise noted.

BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.01	654	YES	---
⊞	.015	70	YES	---
⌀	.02	23	YES	---
⊟	.035	2	YES	---
⊖	.037	18	YES	---
⊡	.041	56	YES	---
⊕	.055	2	YES	---
□	.062	4	YES	---
	.10629921	5	YES	---

Contact person:
Fukun Tang/Electronics Engineer
Electronics Development Group
University of Chicago
Tel: (773)-702-7801, Fax: (773)-702-2971

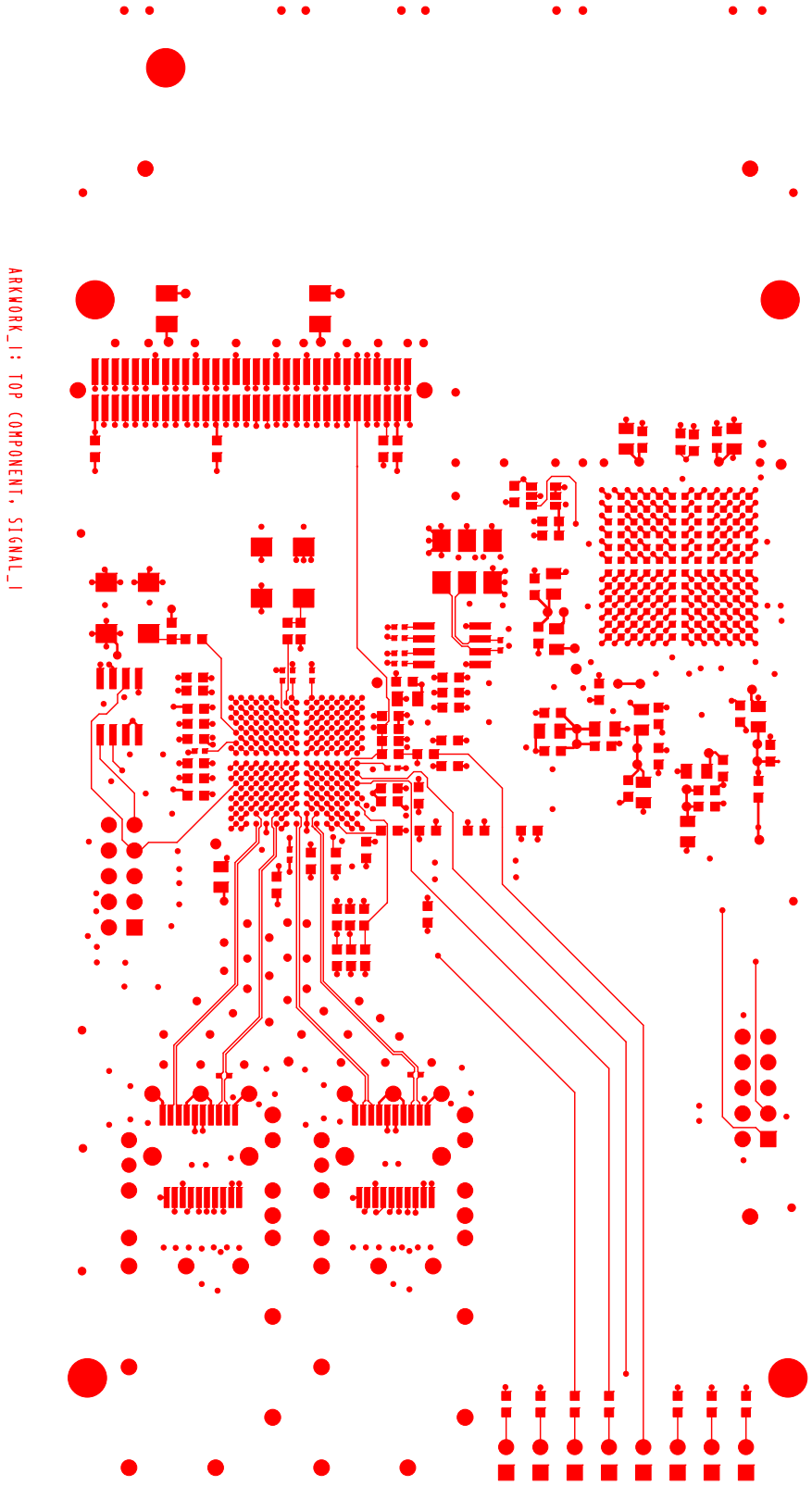
SCH# B2713
SPC# B2714
ASM# B2715

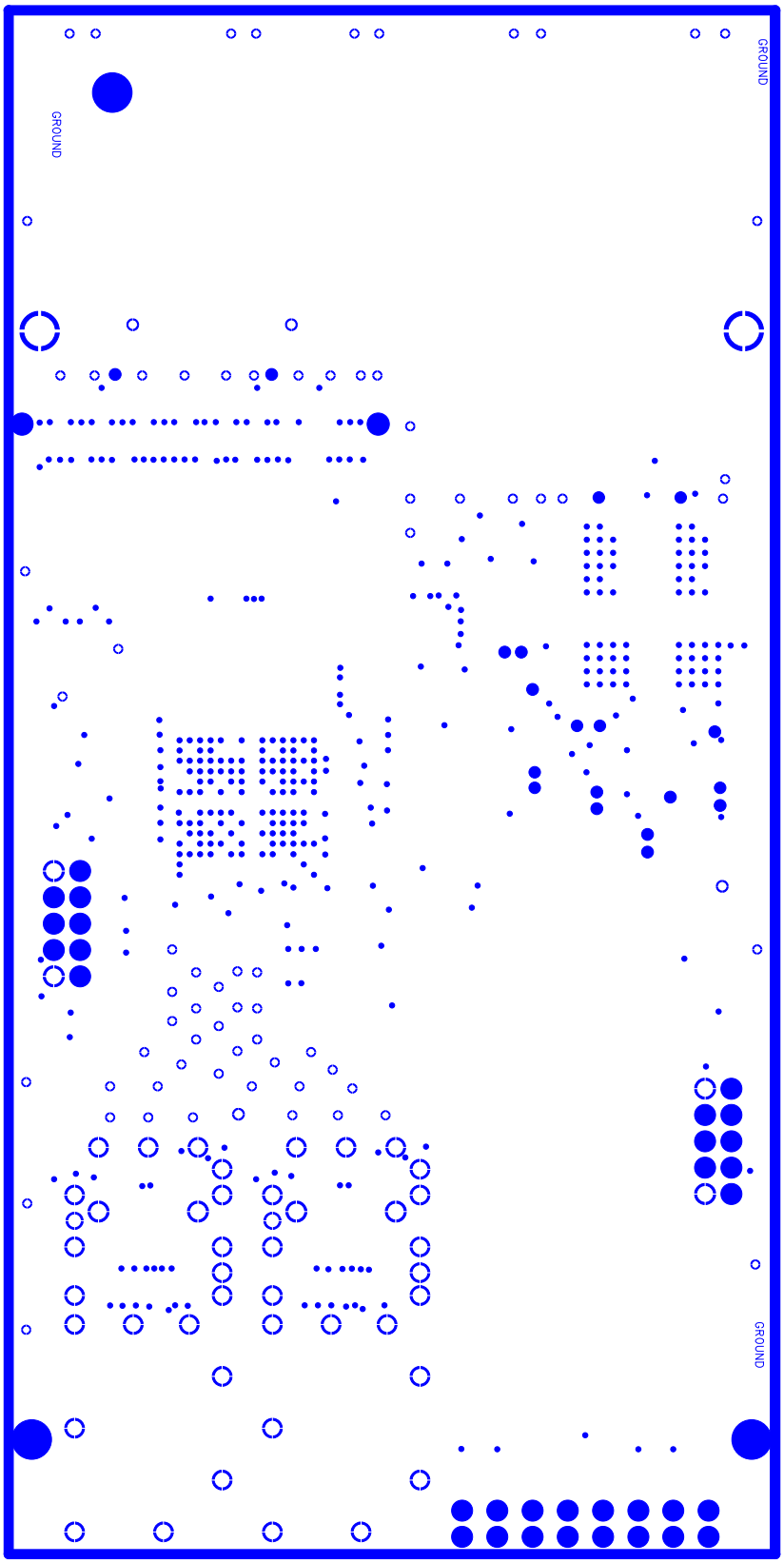
UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
B2714 specifications

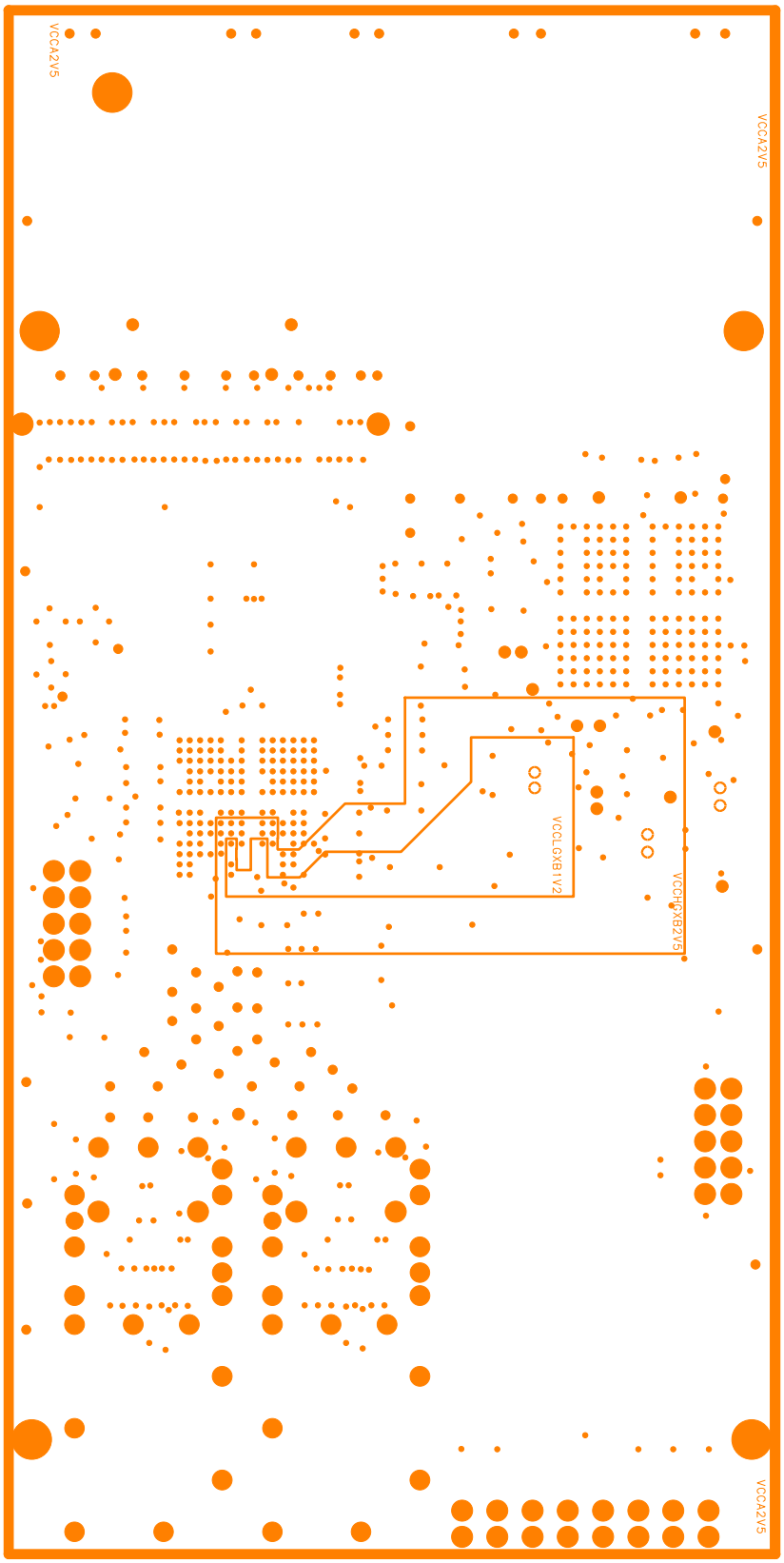
SHEET 1 OF 1
DATE 01/21/2011
DRAWN TANG

B- 2714
REV 1.0

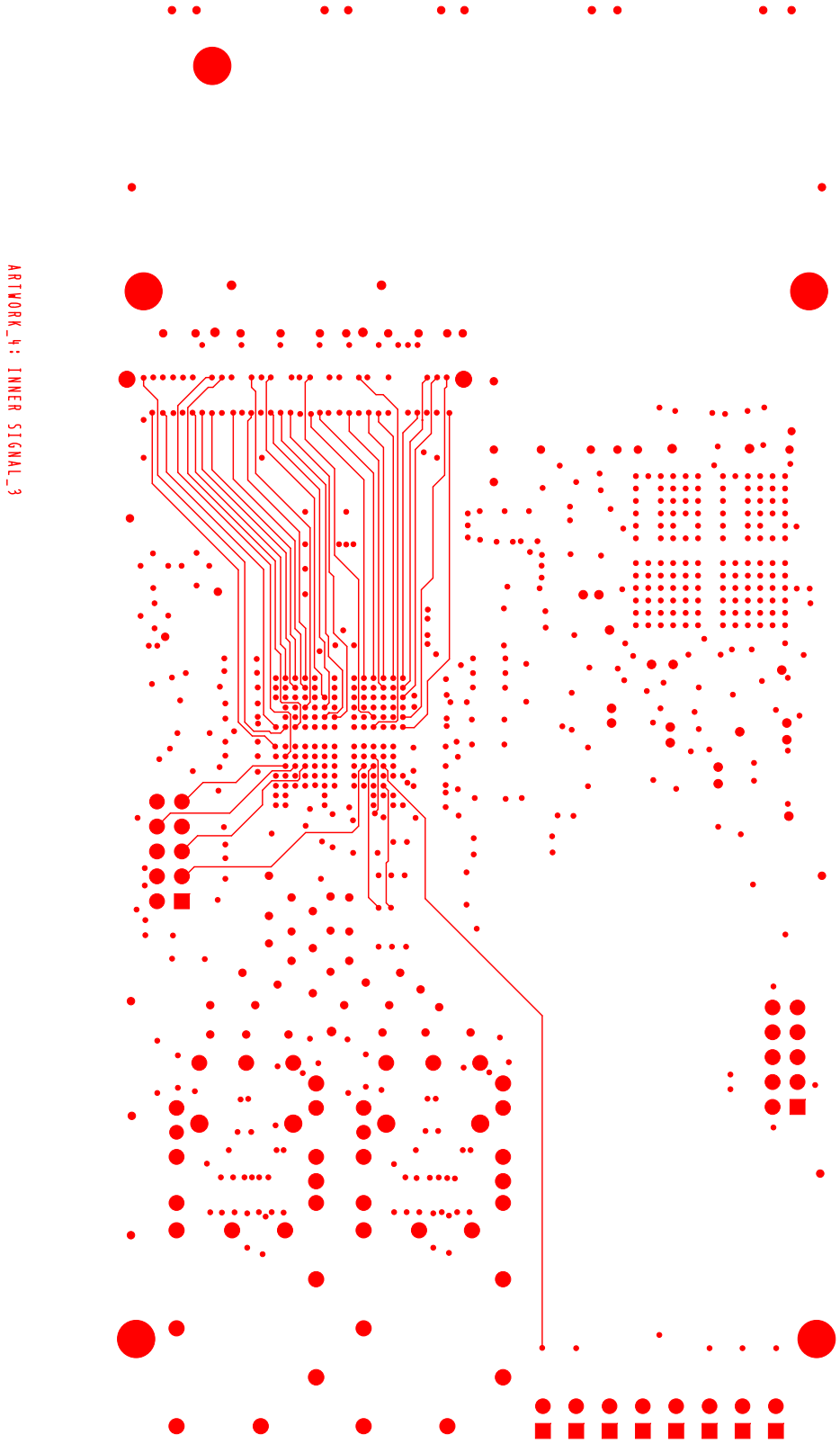

ARKWORK_1: TOP COMPONENT, SIGNAL_1

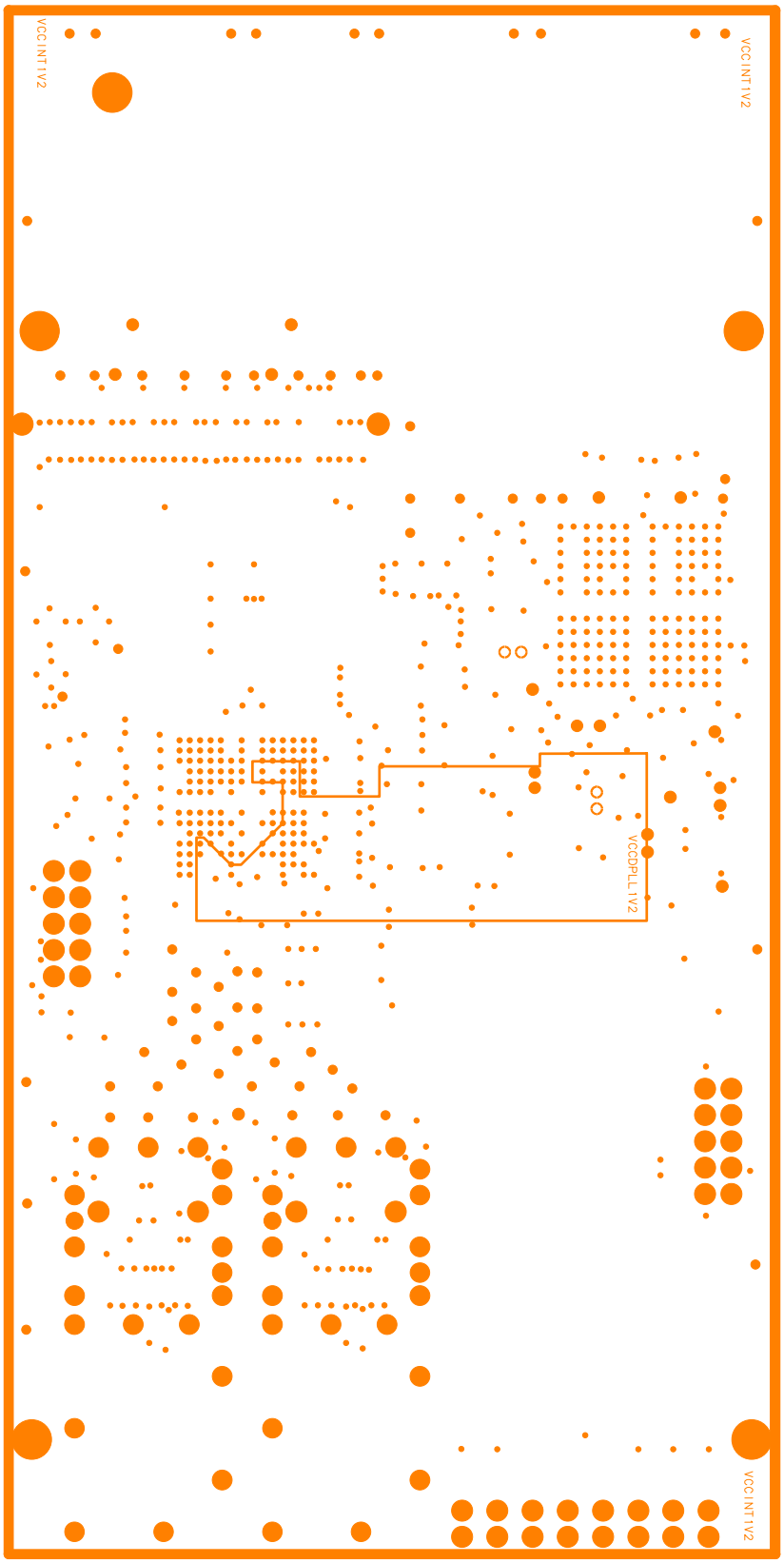


ARTWORK_2: POWER_1: GROUND



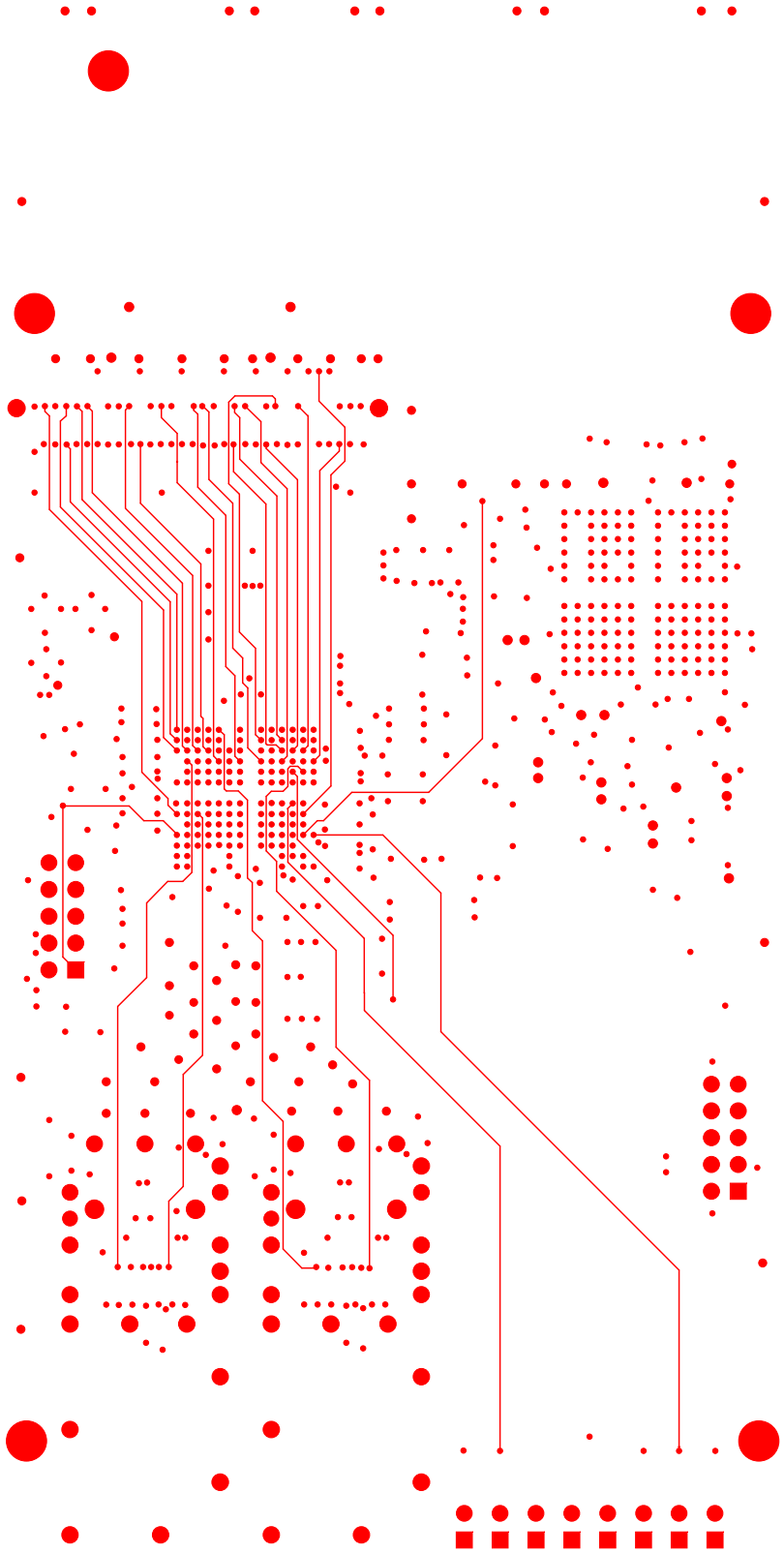
ARTWORK_3: POWER_2,POWER_3, POWER_4 : VCCA2V5,VCCHGXB2V5,VCCLGXB1V2

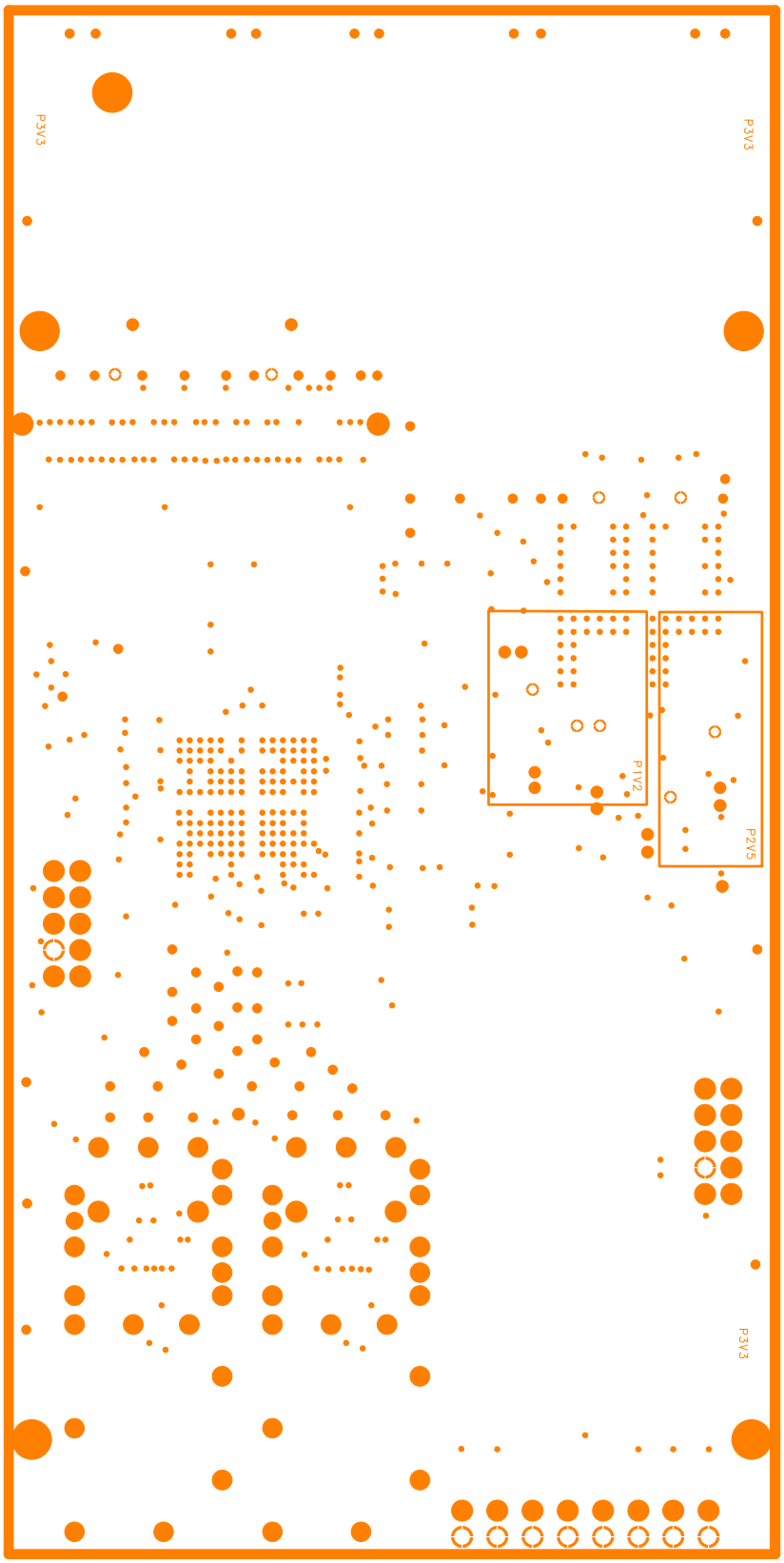

ARTWORK_4: INNER SIGNAL_3



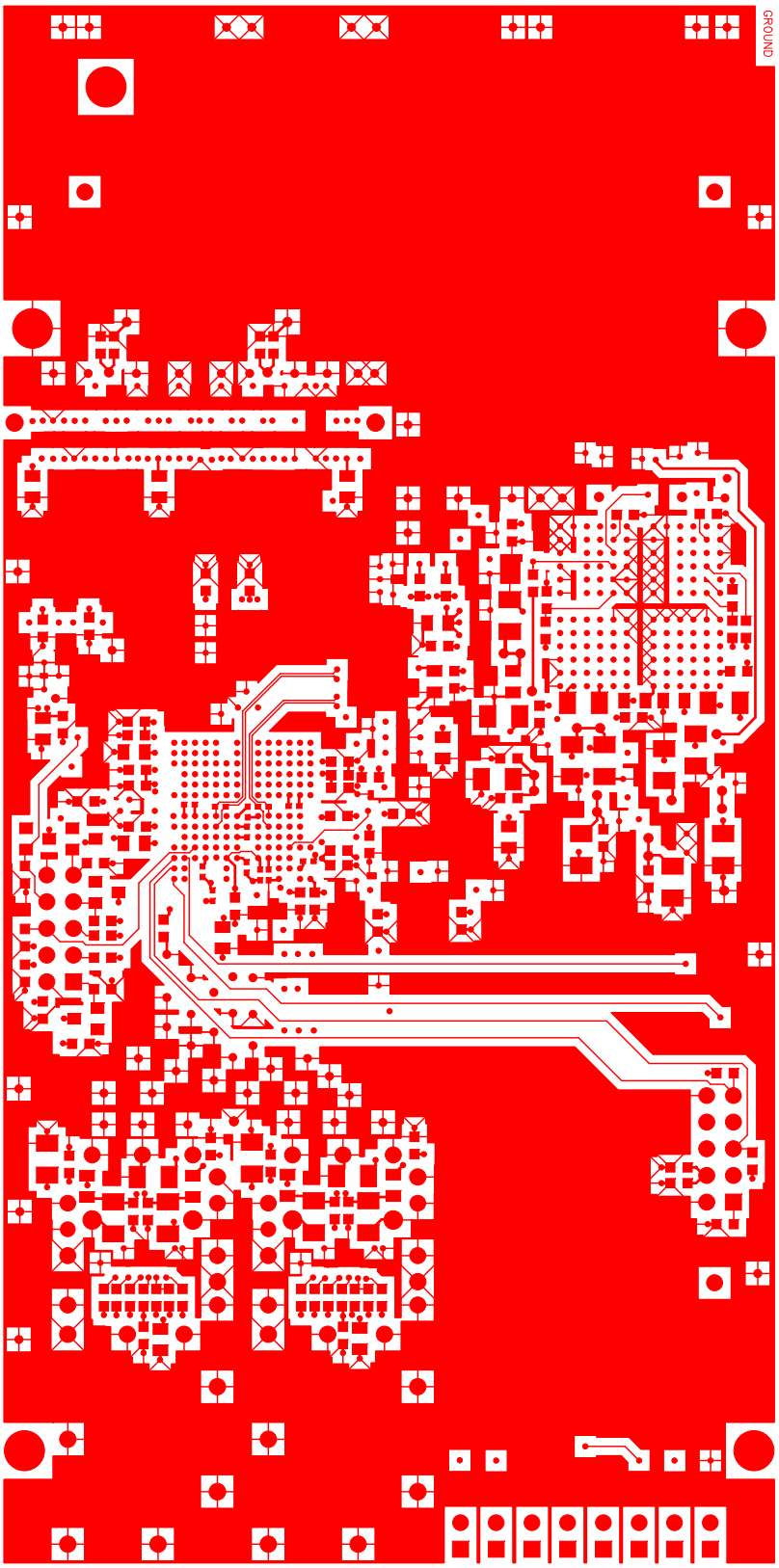
ARTWORK_5: POWER_5, POWER_6: VCCINT1V2, VCCDPLL1V2

ARTWORK_6: INNER SIGNAL_4

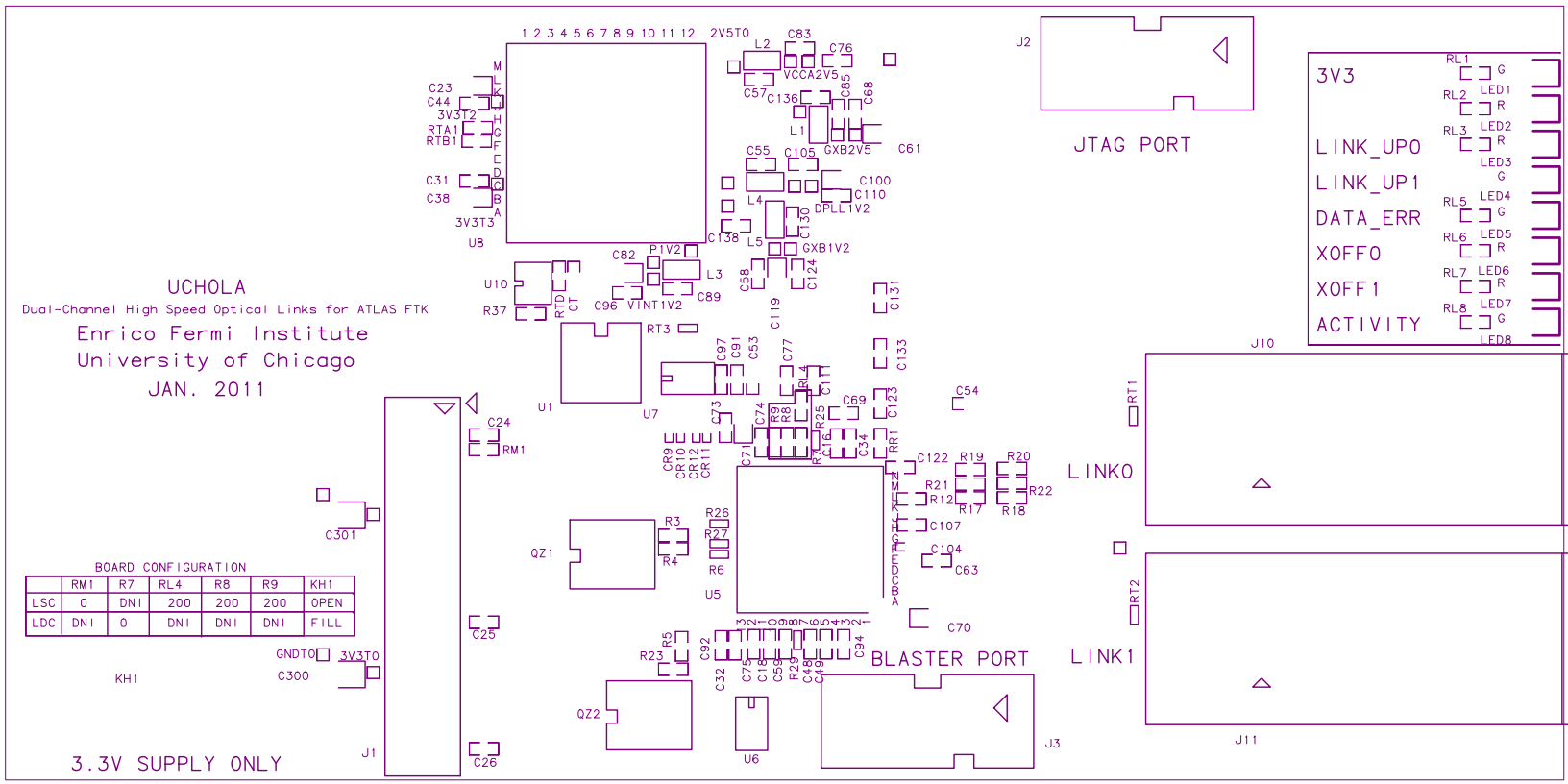




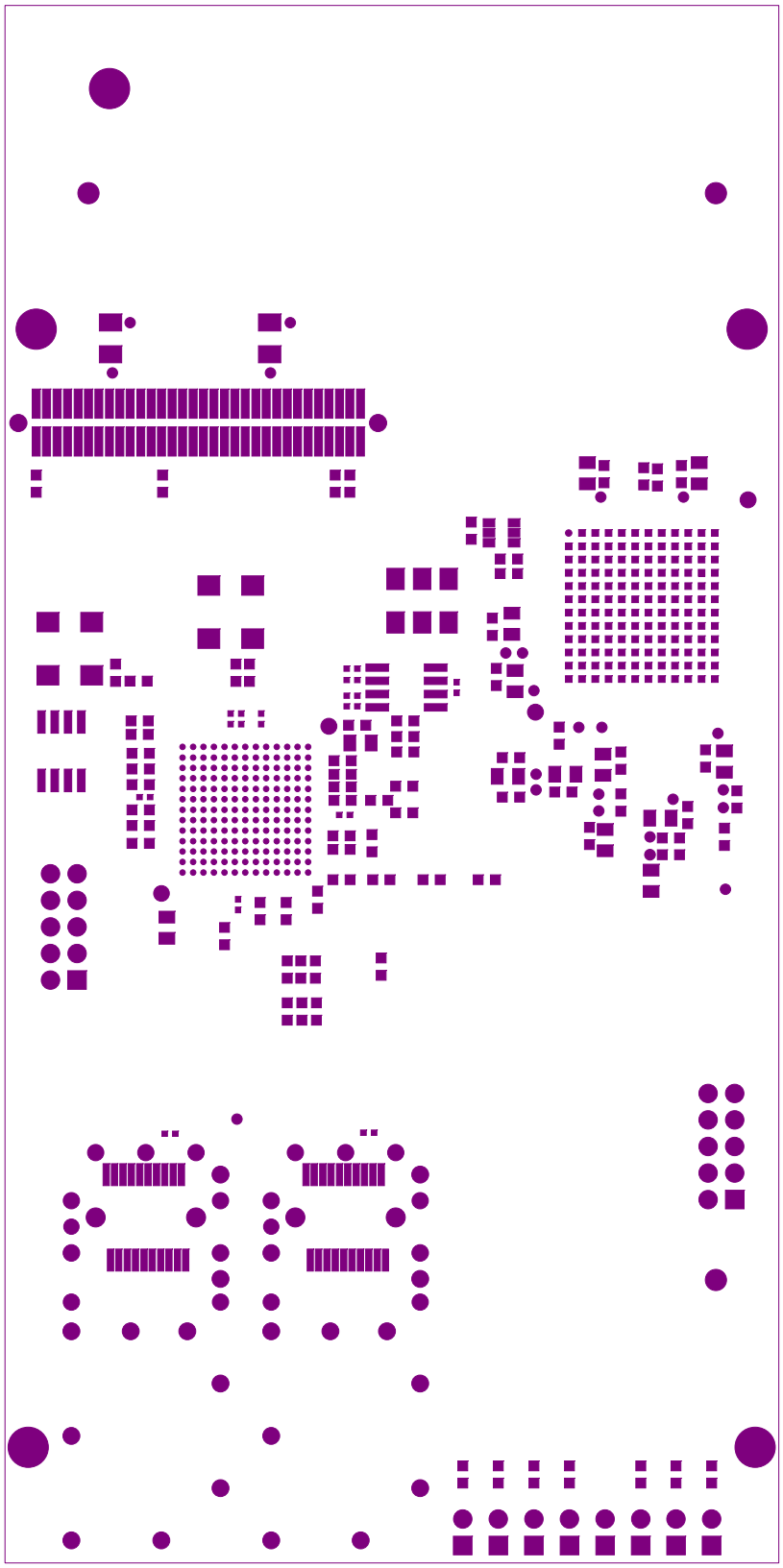
ARTWORK_7: POWER_7, POWER_8, POWER_9: P3V3,P2V5,P1V2



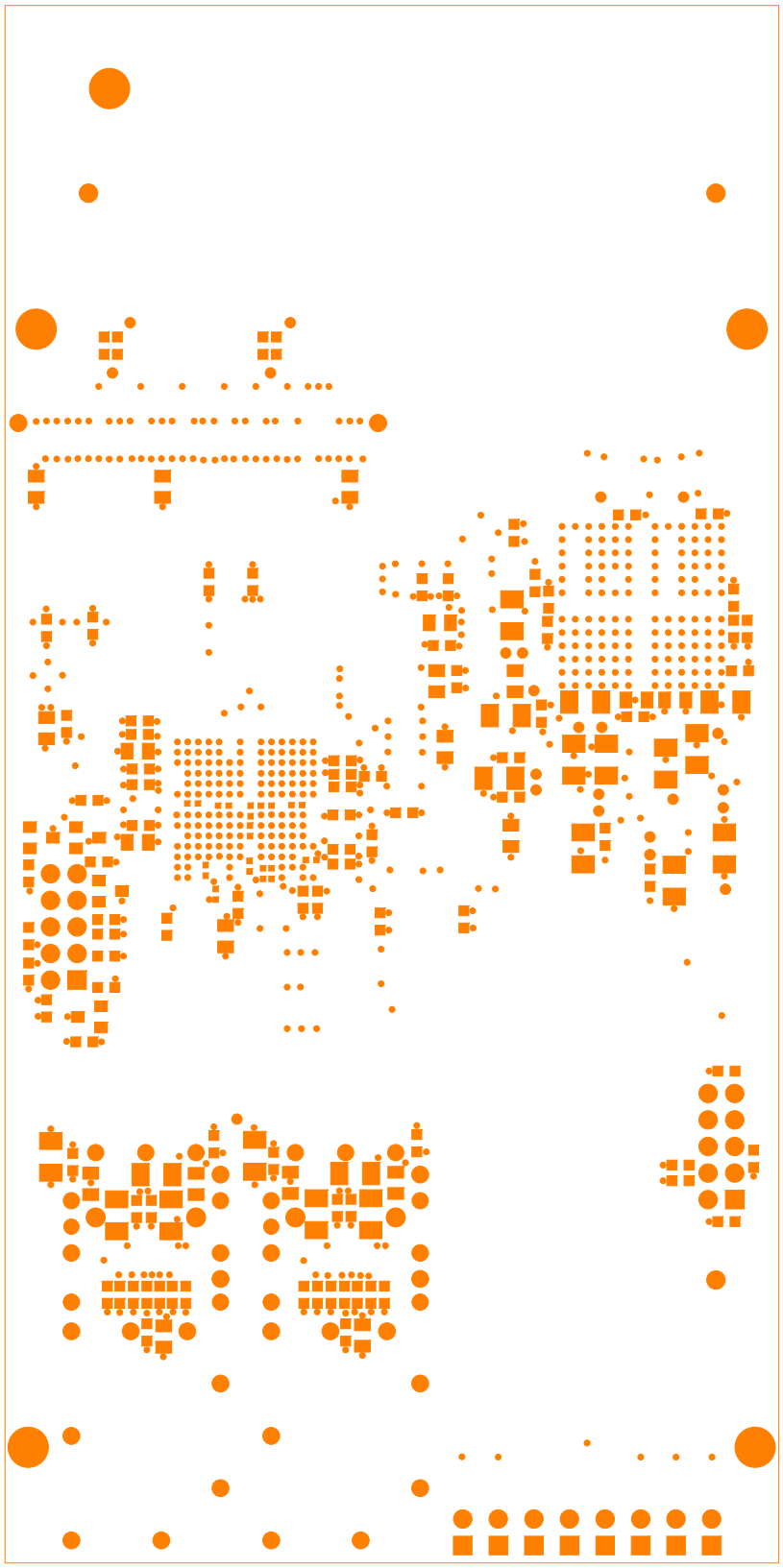
ARKWORK_8: BOTTOM COMPONENT, SIGNAL_2



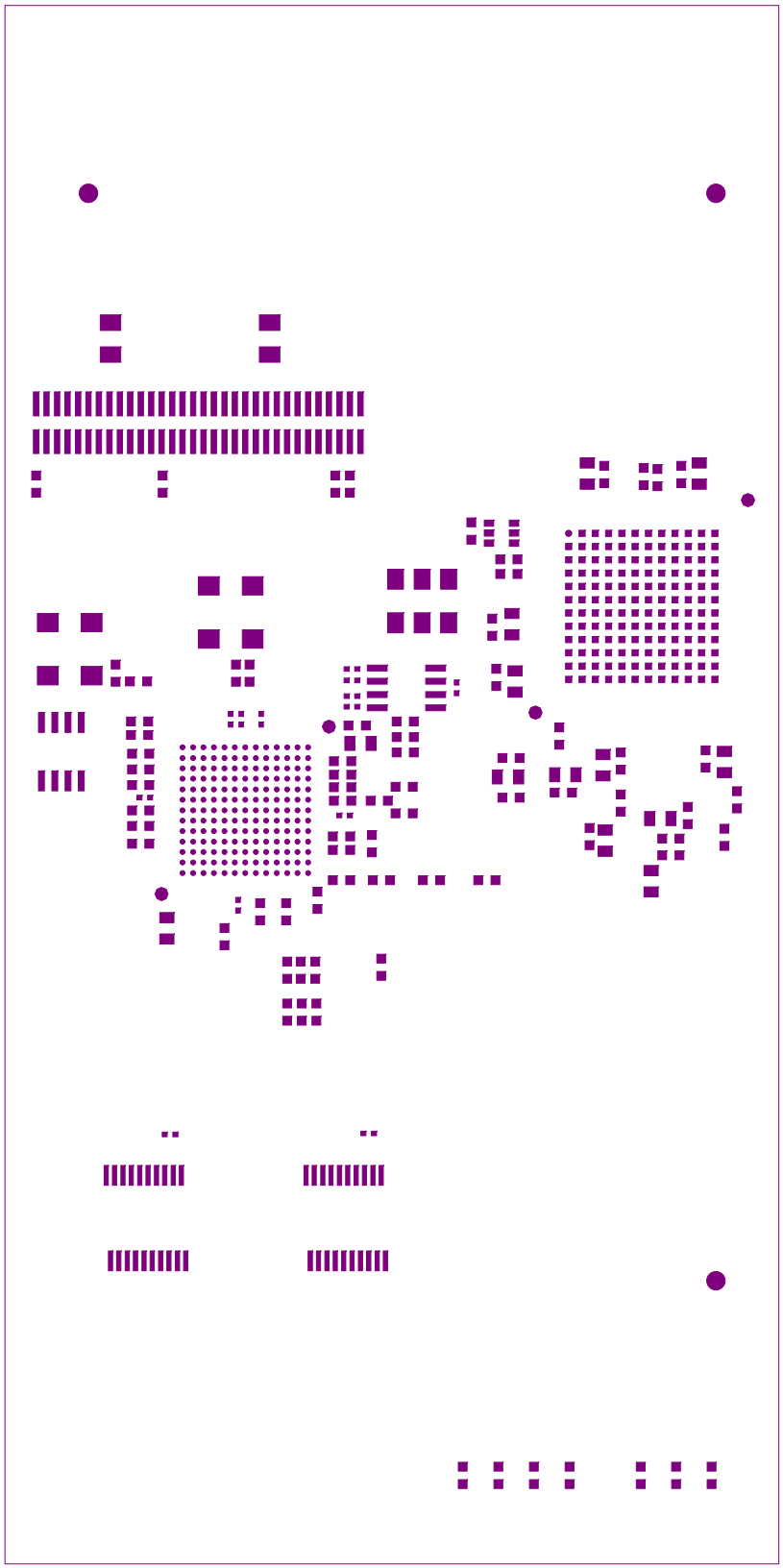
ARTWORK_10: BOTTOM SILKSCREEN



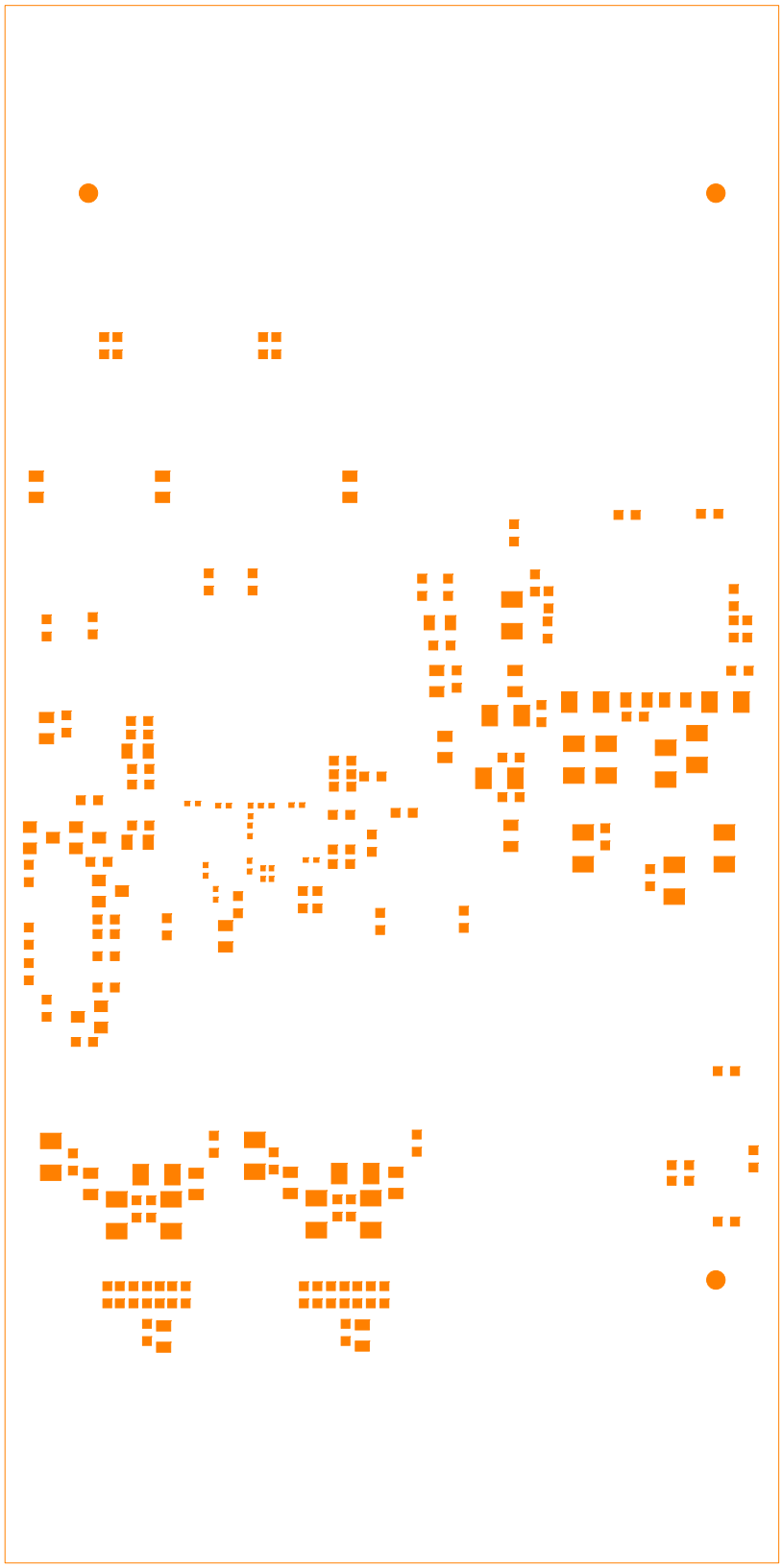
ARTWORK_11: TOP SOLDER MASK



ARTWORK_12: BOTTOM SOLDER MASK

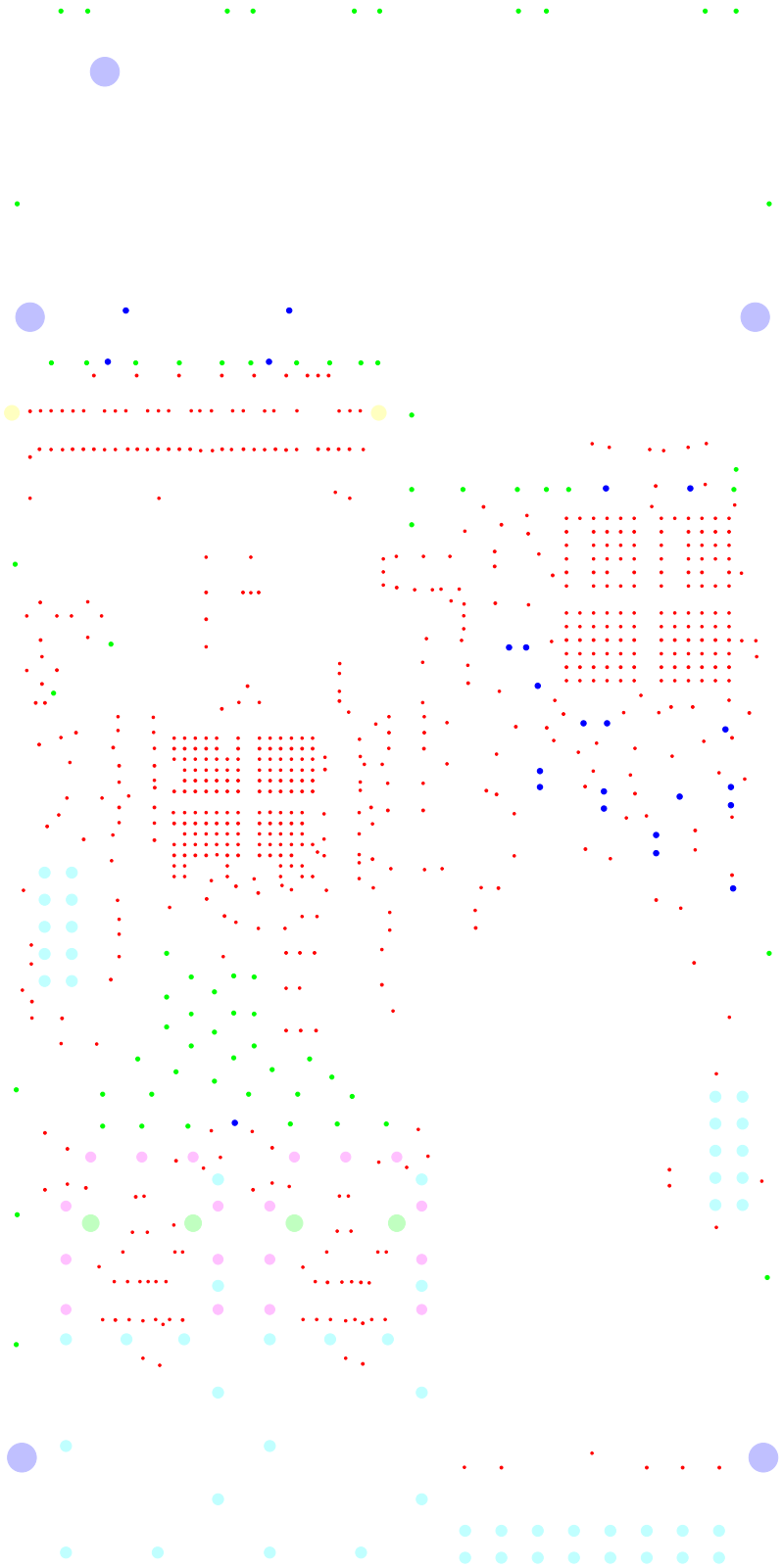


ARTWORK_13: TOP SODER PASTE



ARTWORK_14 BOTTOM SODER PASTE

CAM350 V 10.2.1 : Wed Feb 23 14:26:30 2011 - B2713.cam : drill_plt_unplt



CAM350 V 10.2.1 : Wed Feb 23 14:26:30 2011 - B2713.cam : milling