Dual HOLA Design for FTK Project

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Presentation for Dual HOLA Board Design Review

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Brief Design Specification:
Data Input at Data Port: 32b@40MHz = 1.28Gbps
Data output to Serdes: 32b@50MHz = 1.6Gbps
Line Rate of Optical Links (with 8B/10B) = 2.0Gbps

Link1 (to ATLAS DAQ):
  Full S-Link protocol implemented on transceiver.

Link2 (to FTK):
  Transmitter: Full S-Link protocol implementation
  Receiver: Only “Flow Control” used.

Number of Dual HOLA card in production: 250
6 LV Powers required for FPGA:
• P3V3
• VCCA2V5
• VCCINT1V2
• VCCLGXB1V2
• VCCHGXB2V5
• VCCDPLL1V2
UCHOLA Schematic (2/6 – FPGA Configuration)

- Serial EPROM Configuration (EPCS4)
Schematic (3/6 --- S-Link Data Port & FPGA IOs)

- Slink Data Port and FPGA I/Os
- Power_on Reset
- 50MHz Transceiver Reconfig. Clock
UCHOLA Schematic (4/6 ---Clocks & Optical Transceivers)

- Optical Transceivers
- Transceiver Reference Clock Generators

DC COUPLING: CR9, CR10, CR11, CR12: 0-ohm
• LV DC/DC Module
• 3.3V to 2.5V
• 3.3V to 1.2V
UCHOLA Schematic (6/6—Low Voltage Powers)

- LV Decoupling
Stack-up and trace routing are designed for the best signal integrity

**UCHOLA Board: Layer Stack-up**

<table>
<thead>
<tr>
<th>Artwork#</th>
<th>Physical Layer Name</th>
<th>Logical Signal Name</th>
<th>Plane Integrity</th>
<th>Routing Control</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Art1/L1</td>
<td>Top</td>
<td>Signal_1, Pad_1</td>
<td></td>
<td>Horizontal</td>
<td>(1), (5)</td>
</tr>
<tr>
<td>Art2/L2</td>
<td>Power_1</td>
<td>GROUND</td>
<td></td>
<td>Full Plane</td>
<td></td>
</tr>
<tr>
<td>ART3/L3</td>
<td>Power_2, Power_3, Power_4</td>
<td>VCCA2V5, VCCHGXV2V5, VCCLGXB1V2</td>
<td>Split Plane</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ART4/L4</td>
<td>Inner Signal_3</td>
<td>Signal_3</td>
<td></td>
<td>Horizontal</td>
<td>(2), (4), (6)</td>
</tr>
<tr>
<td>ART5/L5</td>
<td>POWER_5, POWER_6</td>
<td>VCCINIT1V2, VCCDPLL1V2</td>
<td>Split Plane</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ART6/L6</td>
<td>Inner Signal_4</td>
<td>Signal_4</td>
<td></td>
<td>Horizontal</td>
<td>(2), (4), (6)</td>
</tr>
<tr>
<td>ART7/L7</td>
<td>POWER_7, POWER_8, POWER_9</td>
<td>P3V3, P2V5, P1V2</td>
<td>Split Plane</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ART8/L8</td>
<td>Bottom</td>
<td>Signal_2, Pad_2</td>
<td></td>
<td>Vertical</td>
<td>(3), (4), (5)</td>
</tr>
</tbody>
</table>

(1): No fast signal crosses the split gaps on the referenced power layers (for 2.5Gbps CML differential signals)

(2): No fast signal crosses the split gaps on the referenced power layers (for 40Mbps TTL Signals)

(3): No fast signal crosses the split gaps on the referenced power layers (for 100MHz LVDS differential signals)

(4): Filled with "ground" to help reduce inductance in signal return paths and increase thermal conduct for uModule

(5): 100-ohms +/-5% for differential signals on top/bottom layers

(6): 50-ohm +/-5% for single-ended signals on inner signals layers
Dual HOLA Prototype PCB (Top View)

Board Size: 149 x 74mm
Dual HOLA Prototype PCB (Bottom View)

Board Size: 149 x 74mm
Static & BERT Tests

- Low power consumption: $0.62A@3.3V$ (2 Watts Total) with 2 optical transceivers.
- **BERT**: Error free with $1.35E15$ data tested for dual channels.
- **Test setup**: With CERN’s PCI/HOLA test setup, a 7db multimode 850nm attenuator is inserted in each optical fiber for both transmitters and receivers.
- See Anton’s report for details
Two modifications have been made from the prototype board:

1. Incorporating with S-link HW specification, move two optical transceivers 10mm to the right edge of the card.

2. Disconnect Power-on Reset Enable signal from 1.2V power supply.
These 2 connectors will not be installed in production version.

Component height clearance area

41mm
Slink HW specification: 31mm from the right edge of the board

Prototype card violates S-link clearance specification by extending optical transceivers 10mm inside the card!
• We did not see any noticeable affects on the signal integrity from SI simulation by moving the optical transceivers 10mm to the right edge of the board. (FPGA transceivers now only drive differential lines of 31mm with a rate of 2Gbps. (21mm in the prototype card).
Removing “Power_good” (1.2V) Enable Signal

1.2V is not high enough to enable “power-on RESET”. 
We disconnected it in prototype card test.  
(pin-3 has internal pull-up)

No connection to 1.2V in the production boards

Above change will not affect any functional performance!
Summary

• Approval of Production Run
• Purchase order of PCB/Components
• PCB assembly
• Production board tests
• Special thanks to Stefan Haas of CERN for his constant supports and advices on the schematics and PCB designs, as well as test setups. Also thank him for providing us HOLA source and test bench firmware codes.

• Thank Ted Liu of Fermilab for his very valuable advices on the Dual HOLA prototype board tests.

• Thank many others including Arrow Electronics and Altera technical support teams for the valuable discussions and assistances for the FPGA timing model simulations.