B2527 BOARD SPECIFICATIONS

1. Board Layers: 6
2. Layer Stock Order:
Layer 1 (Artwork_1): Top component layer (Signal_1), 1 oz, Z(diff)=100 ohm
Layer 2 (Artwork_2): Power_4 (GROUND), 1 oz
Layer 3 (Artwork_3): Power_2/POWER_3 (P2V5/P1V8), 1 oz
Layer 4 (Artwork_4): Power_1 (P3V3), 1 oz
Layer 5 (Artwork_5): Power_4 (GROUND), 1 oz
Layer 6 (Artwork_6): Bottom component layer (signal_2), 1 oz, Z(diff)=100 ohm

3. Apply silkscreen on both side:
   Artwork_7: Top silkscreen,
   Artwork_8: Bottom silkscreen

4. Apply solder mask over bare copper on both side:
   Artwork_9: Top solder mask
   Artwork_10: Bottom solder mask

5. Material: FR4
6. Board thickness: 0.062" +/- 0.010.
7. Send me layer thickness specification for impedance verification
8. Copper thickness 1 oz before plating for all the power planes.
9. Copper thickness 1 oz before plating for all the signal layers.
10. Ni/Au plating (3 to 8 micro-inches soft gold) over bare copper
11. Differential pairs: trace width/gap=7/7 mils
12. All differential pairs impedance Z(diff) controlled at 100 ohm (+/-10%)
13. All other traces minimum clearance = 7 mils
14. All dimensions are in inches unless otherwise noted.

Contact person:
Fukun Tang/Electronics Engineer
Electronics Development Group
University of Chicago
Tel: (773)-702-7801, Fax: (773)-702-2971
SCH# B2526
SRC# B2527
ASM# B2528

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP
TITLE B2527 specifications
SHEET 1 OF 1
DATE 07/20/2003
DRAWN TANG
REV 1.0