3.3V, 2.5Gbps ANY INPUT-to-LVPECL DUAL TRANSLATOR

FEATURES

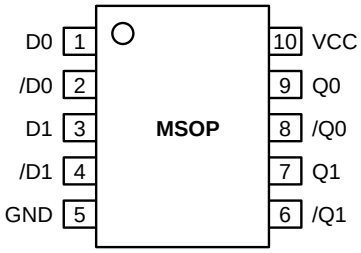
- Input accepts virtually all logic standards
  - Single-ended: SSTL, TTL, CMOS
  - Differential: LVDS, HSTL, CML
- Guaranteed AC parameters over temperature:
  - f_{MAX} > 2.5Gbps (2.5GHz toggle)
  - t_r / t_f < 200ps
  - Within-device skew < 50ps
  - Propagation delay < 400ps
- Low power: 46mW/channel (typ)
- 3.0V to 3.6V power supply
- 100K LVPECL outputs
- Flow-through pinout and fully differential design
- Two channels in a 10-pin (3mm × 3mm) MSOP package

SuperLite™

DESCRIPTION

The SY55857L is a fully differential, high-speed dual translator optimized to accept any logic standard from single-ended TTL/CMOS to differential LVDS, HSTL, or CML and translate it to LVPECL. Translation is guaranteed for speeds up to 2.5Gbps (2.5GHz toggle frequency). The SY55857L does not internally terminate its inputs, as different interfacing standards have different termination requirements.

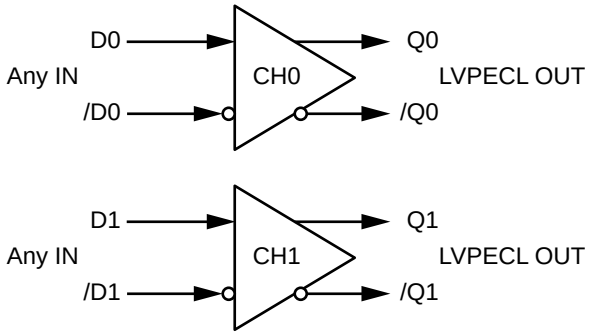
PIN CONFIGURATION



APPLICATIONS

- High-speed logic
- Data communications systems
- Wireless communications systems
- Telecom systems

FUNCTIONAL BLOCK DIAGRAM



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Rev.: B Amendment: /0
Issue Date: March 2003

PIN DESCRIPTIONS

Pin Number	Pin Name	Description
D0, /D0	1, 2	Channel 0 differential inputs (clock or data). See Figure 1 for input structure. See “Input Interface” section for typical interface recommendations.
D1, /D1	3, 4	Channel 1 differential inputs (clock or data). See Figure 1 for input structure. See “Input Interface” section for typical interface recommendations.
Q0, /Q0	9, 8	Channel 0 differential 100k compatible LVPECL outputs. Terminate to V_{CC} – 2V. See “LVPECL Output Termination” section. Outputs are low impedance, emitter-followers. For AC-coupled applications, a pull-down resistor is required on Q and /Q to ensure a DC current path to GND.
Q1, /Q1	7, 6	Channel 1 differential 100k compatible LVPECL outputs. Terminate to V_{CC} – 2V. See “LVPECL Output Termination” section. Outputs are low impedance, emitter-followers. For AC-coupled applications, a pull-down resistor is required on Q and /Q to ensure a DC current path to GND.
GND	5	Device ground. Typically connected to Logic ground.
V_{CC}	10	Supply Voltage. Typically connect to +3.3V ± 10% supply. Bypass with 0.01µF//0.1µF low ESR capacitors.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

Do not leave unused inputs floating. Tie either the true or complement inputs to ground, but not both. A logic zero is achieved by connecting the complement input to ground with the true input floating. For a TTL input, tie a 2.5kΩ resistor between the complement input and ground. See “Input Interface” section.

Input Levels

LVDS, CML and HSTL differential signals may be connected directly to the D inputs. Depending on the actual worst case voltage seen, performance of SY55857L varies as per the following table:

Input Voltage Range	Minimum Voltage Swing	Maximum Translation Speed
0 to 2.4V	100mV	2.5Gbps
0 to V_{CC} +0.3	200mV	1.25Gbps

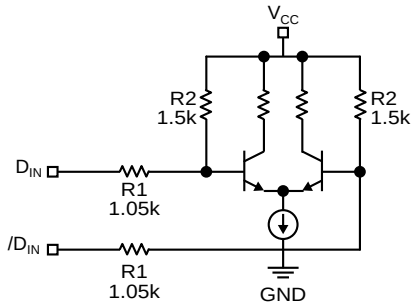


Figure 1. Simplified Input Structure

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{CC}	Power Supply Voltage		–0.5 to +6.0	V
V_{IN}	Input Voltage		–0.5 to V_{CC} +0.5	V
I_{OUT}	Output Current	–Continuous –Surge	50 100	mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{store}	Storage Temperature Range		–65 to +150	°C
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient)	–Still-Air –500lfpm	113 96	°C/W °C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case)		42	°C/W

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS[1]

T_A = –40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage[2]	3.0	3.3	3.6	V	
I_{CC}	Power Supply Current[2]	—	28	45	mA	Inputs/Outputs Open

Note 1. Specification for packaged product only.

Note 2. The specifications shown above are valid after thermal equilibrium has been established.

INPUT ELECTRICAL CHARACTERISTICS[1, 2]

V_{CC} = 3.0V to 3.6V; GND = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{ID}	Differential Input Voltage	100	—	—	mV	V_{IN} < 2.4V
		200	—	—	mV	V_{IN} < V_{CC}+0.3V
V_{IH}	Input HIGH Voltage	—	—	V_{CC}+0.3V	mV	
V_{IL}	Input LOW Voltage	–0.3	—	—	mV	

Note 1. Specification for packaged product only.

Note 2. The specifications shown above are valid after thermal equilibrium has been established.

(100K) LVPECL OUTPUT CHARACTERISTICS[1, 2]

V_{CC} = 3.0V to 3.6V; GND = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OL}	Output LOW Voltage	1355	1480	1605	mV	50Ω to V_{CC}–2V
V_{OH}	Output HIGH Voltage	2155	2280	2405	mV	50Ω to V_{CC}–2V
V_{SWING}	Output Voltage Swing	600	700	—	mV_{p-p}	50Ω to V_{CC}–2V

Note 1. Specification for packaged product only.

Note 2. 100K circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at V_{CC} = 3.3V. They vary 1:1 with V_{CC}.

AC ELECTRICAL CHARACTERISTICS[1, 2]

V_{CC} = 3.0V to 3.6V; GND = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{MAX}	Maximum Frequency NRZ Data Clock[3]	2.5 2.5	— —	— —	Gbps GHz	small signal, V_{IN} < 2.4V
	NRZ Data Clock[3]	1.25 1.25	— —	— —	Gbps GHz	large signal, V_{IN} < V_{CC}+0.3V
t_{PLH} t_{PHL}	Propagation Delay (Differential) D0 to Q0, D1 to Q1	—	—	400	ps	
t_{SKEW}[4]	Within-Device Skew (Diff.) Part-to-Part Skew (Diff.)	— —	— —	50 200	ps	
t_{JITTER}	Jitter Generation (rms)		<1		ps (rms)	
t_r , t_f	PECL Output Rise/Fall Times (20% to 80%)	—	—	200	ps	

Note 1. Specification for packaged product only.

Note 2. Performance is guaranteed as shown in the above table after thermal equilibrium has been established.

Note 3. Clock frequency is defined as the maximum toggle frequency, and guaranteed for functionality only. Measured with a 750mV signal, 50% duty cycle. All loading is with a 50W to V_{CC} – 2V.

Note 4. Skew is measured between outputs under identical transitions.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	Package Marking
SY55857LKI	K10-1	Industrial	857L
SY55857LKITR*	K10-1	Industrial	857L

*Tape and Reel

INPUT INTERFACE

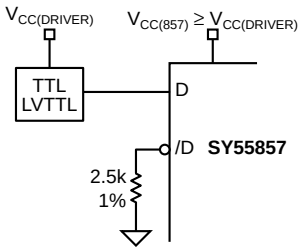


Figure 1. 5V, 3.3V "TTL"

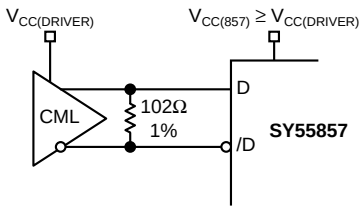


Figure 2. CML-DC Coupled

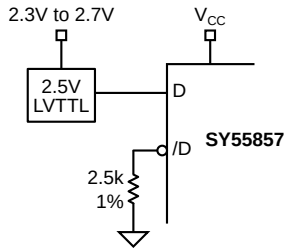


Figure 3. 2.5V "TTL"

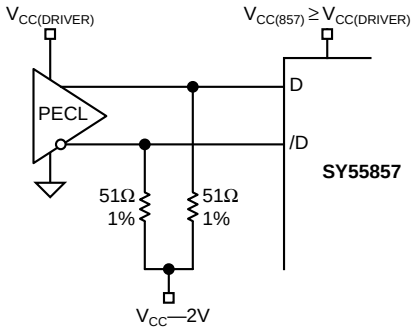


Figure 4. PECL-DC Coupled

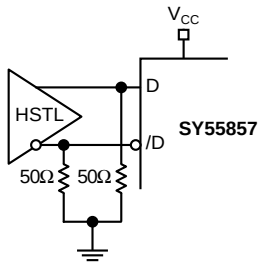


Figure 5. HSTL

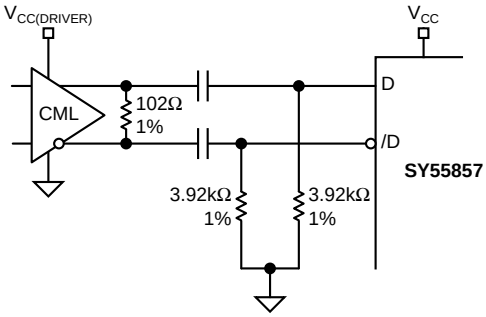


Figure 6. CML-AC Coupled - Short Lines

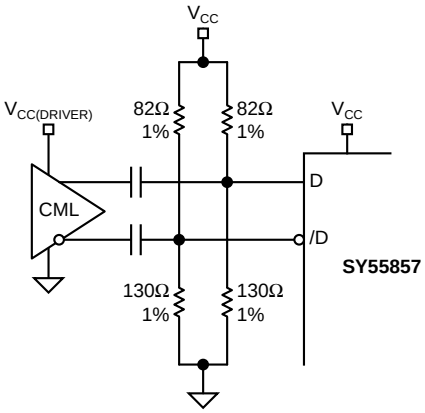


Figure 7. CML-AC Coupled - Long Lines

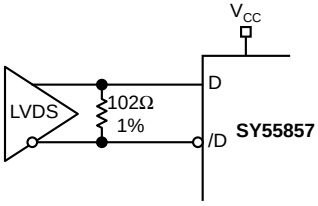


Figure 8. LVDS

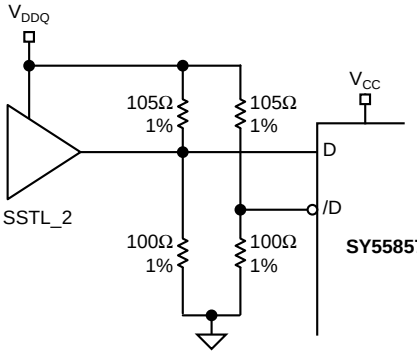


Figure 9. SSTL_2

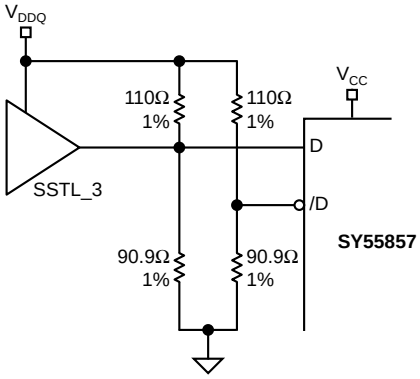
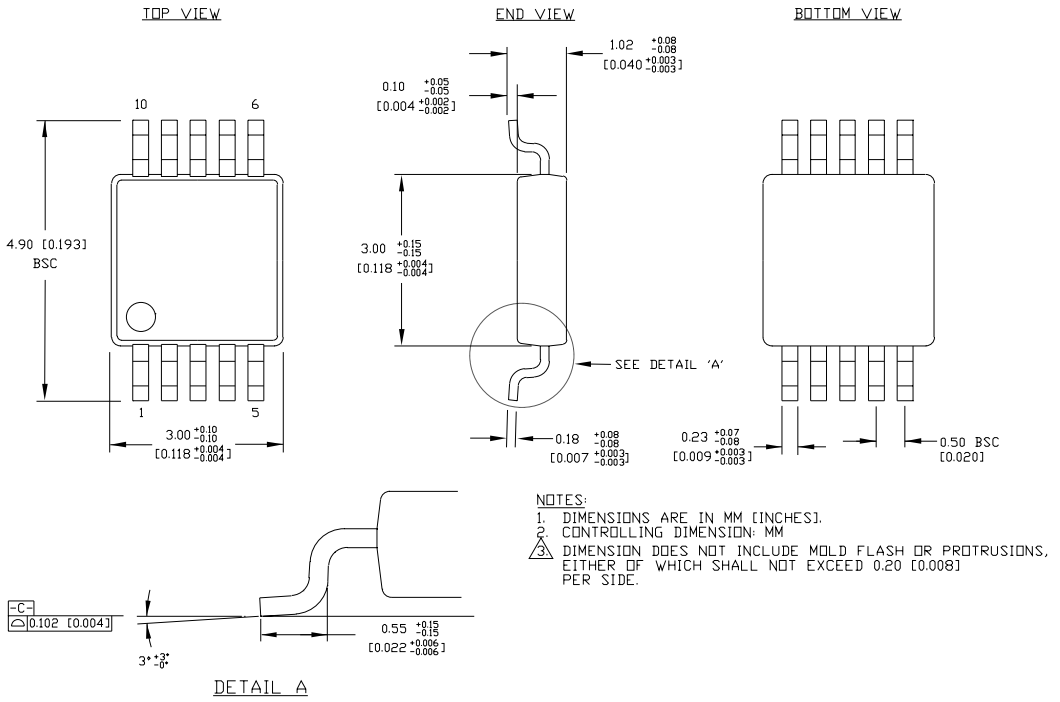


Figure 10. SSTL_3

10 LEAD MSOP (K10-1)



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