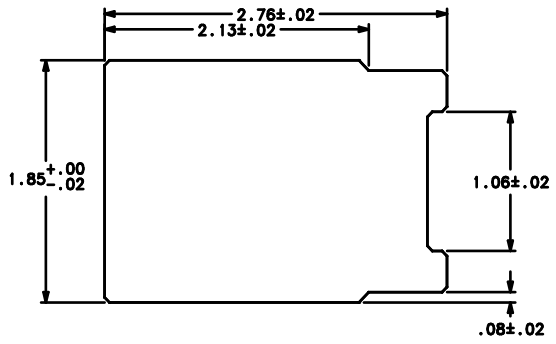
B2829 PCB SPECIFICATIONS



1. Board Layers: 6
2. Layer Stack Order:

ARTWORK_1: Top Component Layer (Signal_1, PAD_1), 1oz.
ARTWORK_2: POWER PLANE (AGND), 1oz.
ARTWORK_3: POWER PLANE (VCC), 1oz.
ARTWORK_4: POWER PLANE (VEE), 1oz.
ARTWORK_5: POWER PLANE (GROUND), 1oz.
ARTWORK_6: Bottom Side Layer (Signal_2, PAD_2), 1oz.

3. Apply silkscreen on both side:
   - Artwork_7: Top component side silkscreen.
   - Artwork_8: Bottom component side silkscreen.
4. Apply solder mask over bare copper on both side:
   - Artwork_9: Top component side solder mask.
   - Artwork_10: Bottom component side solder mask.
5. Solder paste photo plots for assembly stencils.
   - Artwork_11: Top solder paste mask
   - Artwork_12: Bottom csolder paste mask
6. Material: FR4 with Tg >170C.
7. Board thickness: 0.062' +/- 0.010.
8. All layers use 1 oz copper before plating.
9. Differential trace impedance control at 100 ohms +/- 10%. Trace/gap/trace = 5/5/5 mils
10. Mininum trace/gap = 5/5 mils
11. Ni/Au finish over bare copper.
12. Apply solder mask over bare copper
13. Send back photo plots and layer stack parameters for rechecking.
14. All dimensions are in inches unless otherwise noted.
15. Milling data file is provided for board cutting.

BOARD's DRILL SCHEDULE (Inch)

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
O	.015	234	YES	---
⊞	.02	25	YES	---
⊙	.035	43	YES	---
⊟	.041	6	YES	---
⊖	.059	6	YES	---

16: Contact person:
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SCH# B2829 V1.0
SPC# B2830 V1.0
ASM# B2831 V1.0

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
B2829 Specification Drawing

SHEET 1 OF 1
DATE OCT-1-2013
DRAWN F. Tang

B- 2829
REV 1.0