ATLAS TileCal Demonstrator
Main Board Design Review

Fukun Tang, Kelby Anderson and Mark Oreglia

The University of Chicago
Main/Daughter Board Readout Structure (1/2 board)
A Single PMT Readout Data Flow

**Front-end Board (3-in-1)**
- Analog Trigger
- Analog low gain
- Analog high gain
- Analog Integrator

**Analog Summing Board**
- Trigger Sum

**ADC (low gain)**
- Low gain ADC data
- Data frame
- Data clock

**ADC (Hi Gain)**
- High gain ADC data

**Control Unit**
- Integrator ADC I²C Bus
- Integrator ADC data

**Fast Signal Processing**
- 2-ch ADC Serial Bus
- SPI Bus & Timing

**Slow Signal Processing**
- Bus to 3 FEC for control and timing

**FPGA (Cyclone IV)**
- SPI Bus & Timing

**To Daughter Board**
- PMT
- Fast Signal Processing
- Slow Signal Processing
12-bit ADCs --- Input Considerations (2-ch is shown)

Input range bias adjustment: pedestal, baseline shift etc.

Differential input + sink

500mV
Vcm=0.9V

Signal from 3-in-1 low gain output:
- 500mV
- 0V
- -500mV

Signal from 3-in-1 high gain output:
- 500mV
- 0V
- -500mV

Sink wire is used for unbalanced current path

ADC: LTC2264-12
Each ADC is readout in serial format @14b x 40MHz = 560Mbps
Every dual ADC shares one DCO
Every ADC in one Region shares one FR

1-Lane Output Mode, 14-Bit Serialization

40MHz

280MHz

40MHz

560Mbps

D2∗ AND D7∗ ARE EXTRA NON-DATA BITS FOR COMPLETE SOFTWARE COMPATIBILITY WITH THE 14-BIT VERSIONS OF THESE ADCS. DURING NORMAL NON-OVERRANGED OPERATION D2∗ AND D7∗ ARE SET TO LOGIC 0. SEE THE DATA FORMAT SECTION FOR MORE DETAILS.
Schematics of Integrator ADCs and Readout (6-ch shown)
12-channel dedicated serial buses to readout high gain and low gain ADCs
   - Each channel has 4 pairs of LVDS signals (SDO0, SDO1, DFRAME, DCK).
4 group of SPI buses connected each FPGA for interfacing MB and DB.
   - Each SPI bus has 4 pairs of LVDS signals (SEL, DI, DO, DCK)
2 group of LVDS charge injection control signals (TPH, TPL, EXC, RESET)
4 group of LVDS I²C buses (SDA, SCL) for Integrator ADC readout
2 group of 2.5V CMOS JTAG signals (TMS, TDI, TDO, TCK)
2 global LVDS Reset signals
6 single-end LV signals (0 to 1VDC) for on board LV monitors (Built-in ADC in Kentex 7)
+10V, +10V_sense, Ground
Reserved signal.

All above signals are defined in 400-pin connector.
• 5 pairs of LVDS signals for integrator gain/cal control (ICAL, S1, S2, S3, S4)
  – 6 valid gain settings and one calibration enable signals
• Two pairs of LVDS signals for charge injection (TPH, TPL)
  – For high gain and low gain charge injections
• 3 pair of LVDS signals for calibration DAC settings (DI, CK, LD)
• One pair of analog integrator output signals.
• +5V, -5V and ground
All Above signals are defined in 40-pin connector mating with ribbon cable.

• 2 pair of analog fast PMT signals (h/L gains)
• One pair of LVDS signals for analog trigger enables.
Main Board Layout Plan

- Physical area: 2 Sections (A & B)
- Logical area: 4 Regions (A0, A1, B0, B1)
FPGA Configurations

- FPGA configurations can be done with one daisy-chained JTAG port in one drawer.
- And have an option to configure FPGAs for each Main Board individually.
Consideration of Power Supply Redundancy

2 independent +10V supplies for each Main Board

Main Board Section-A
- +10V_SEC_A
- +10V_SEC_B
- Fuses
- Local LVs:
  - +10V, +5V, -5V, +2V5
  - +1V8D, +1V8A
  - +1V2, AGND, GND

Main Board Section-B
- +10V_SEC_B
- Local LVs:
  - +10V, +5V, -5V, +2V5
  - +1V8D, +1V8A
  - +1V2, AGND, GND

Xilinx Kintex-7
- FPGA -A
- FPGA -B
- SNAP-12 (PPOD)

12-ch fibers
400-pins conn.
DC/DC Converters

• 2 dual step-down DC/DC converters per Section
  ✓ Input: +10V (accept 4.5V to 26V)
  ✓ Outputs: +5V_A, +2V5_A, +1V8_A, +1V2_A
  ✓ Each switcher 180 degree out of phase for noise and ripple suppression.

• One positive to negative DC/DC converters LT3759 per Section
  ✓ Input: +10V (accept 2.6V to 42V)
  ✓ Output: -5V
- Main Board Dimension: 690x100mm
- 12 Mounting Holes: $\phi = 3.5mm$
  - Mounting holes grounded on PCB for better thermal conducting, it should be insulated to detector ground by alumina posts.

- Daughter Board: 250x100mm
- Summing Adapter Board: 252x100mm
Mainboard Layout View

Complexity and Challenges:
- High speed: (640 Mbps)
- Max. trace length: (20 inches)
- All routes are same direction routes
- Crosstalk consideration: (parallel and tandem)
- Mixed signals (low noise analog and high speed digital)
- Equal timing high speed traces
- Current rate constraints
- Swish-cheesed power planes (via usage limitation)
- Many other challenges such as DC/DC switchers

6 Signal layers
8 Power layers including 3 redundant ground layers (continuous solid plane) for signal integrity and tandem crosstalk reduction

High via and trace density
High via density
Top/Bottom Layers
Typical Inner Signal Layers
Typical Spited Power Layers
Preliminary simulations for early evaluation of signal integrity (1)

Diff. pairs: Top/Bottom layer, 20-inches (100-ohm)
Code: PRBS5 800Mbps
Priliminary simulations for early evaluation of signal integrity (2)

Diff. pairs: Inner layers, 20-inches (100-ohm)
Code: PRBS5 800Mbps
PCB Specifications

- QA Specification: Comply with IPC 6012 Class 2
- Material Glass Transition Temperature: Tg > 170°C
- Do we need IPC 6012 Class 3 qualification?
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Layer Stack-up and Diff. Impedance Evaluation

To/Bot Diff: Z=98.53 ohms

Inner Signal Diff: Z=98.53 ohms

Total Thickness: 91.4 mils
Placement of Functional Blocks on Main Board

Top Side View of Virtual PCB

- Patch Panel (Higher Dose)
- 12 H/L Gain ADC + 3-in-1 Control
- 4 FPGAs for Main/FEC timing and control
- 12-ch Integrator ADCs
- All local LVs Monitor Drivers
- Positive DC/DC Regulators (Components on back)
- 400-pin MD/DB Interconn.
- 10V to -5V DC/DC
- 4 Summing card power conn.
- Local DACs for ADC bias settings
- 12 H/L Gain ADC + 3-in-1 Control
PCB quotes were sent to 7 PCB houses.  
Only 3 PCB quotes received, others say “sorry” since it is an oversized board.

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1200 boards  
No Vendor could bid until they see the yield from the prototype run!

4/24/2013  
Fukun Tang
Thanks you!