B-2800 BOARD SPECIFICATIONS

1. Board Layers: 14
2. Layer Stack Order:
   Layer1 (Artwork_1): Top comp layer (Signal_1) 1 oz, Zdiff=100 ohms
   Layer2 (Artwork_2): Power plane (AGND_A, AGND_B), 2oz
   Layer3 (Artwork_3): Inner Signal_3, 1oz, Zdiff=100 ohms
   Layer4 (Artwork_4): Power plane (Ground), 2oz
   Layer5 (Artwork_5): Power plane (PSV_A, PSV_B), 2oz.
   Layer6 (Artwork_6): Power plane (P10V_A, P10V_B, P1V2_A, P1V2_B), 2oz
   Layer7 (Artwork_7): Power plane (P2V5_A, P2V5_B, P1V8A_A, P1V8A_B), 2oz
   Layer8 (Artwork_8): Power plane (N5V_A, N5V_B), 2oz
   Layer9 (Artwork_9): Inner Signal_4, 1oz, Zdiff=100 ohms
   Layer10 (Artwork_10): Inner Signal_6, 1oz, Zdiff=100 ohms
   Layer11 (Artwork_11): Power plane (Ground), 2oz
   Layer12 (Artwork_12): Bottom comp layer (Signal_2) 1 oz, Zdiff=100 ohms

3. Apply silkscreen on Top component side:
   Artwork_13: Top silkscreen.
   Artwork_14: Bottom silkscreen.

4. Apply solder mask over bare copper on both side:
   Artwork_15: Top solder mask
   Artwork_16: Bottom solder mask

5. Material: FR4, TG > 170C
6. Board thickness: 0.090" +/- 0.010".
7. Diff traces impedance of all signal layers should be controlled at 100 ohms +/-5%.
8. Diff trace/gap/trace laid out in 5/5/5 mils, can be adjusted by PCB makers for impedance control.
9. Minimum Trace/gap = 5/5 mils
10. Copper thickness for signal layers before plating is 1oz.
11. Copper thickness for all power layers is 2oz.
12. Board finish type: immersion gold.
13. Solder masking for all bare copper
14. All dimensions are in inches unless otherwise noted.
15. Send back stack-up parameters and suggested trace/gap for impedance control for approval.
16. Send back gerber plots (pdf is acceptable) for approval.

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If you configure a master device with an SFL design, the master device enters user mode even though the slave devices in the multiple device chain are not being configured. The master device enters user mode with a SFL design even though the CONF_DONE signal is externally held low by the other slave devices in chain. Figure 8–29 shows the JTAG configuration of a single Cyclone IV device with a SFL design.

**Figure 8–29. Programming Serial Configuration Devices In-System Using the JTAG Interface**

![Diagram showing JTAG configuration](image)

**Notes to Figure 8–29:**

1. Connect the pull-up resistors to the VCCIO supply of the bank in which the pin resides.
2. The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL for AS configuration schemes, refer to Table 8–3 on page 8–8, Table 8–4 on page 8–8, and Table 8–5 on page 8–9. Connect the MSEL pins directly to VCCA or GND.
3. Pin 6 of the header is a VIO reference voltage for the MasterBlaster output driver. The VIO must match the VCCA of the device. For this value, refer to the MasterBlaster Serial/USB Communications Cable User Guide. When using the ByteBlasterMV download cable, this pin is a no connect. When using USB-Blaster, ByteBlaster II, and EthernetBlaster cables, this pin is connected to nCE when it is used for AS programming, otherwise it is a no connect.
4. You must connect the nCE pin to GND or driven low for successful JTAG configuration.
5. The nCEO pin is left unconnected or used as a user I/O pin when it does not feed the nCE pin of another device.
6. Power up the VCC of the EthernetBlaster, ByteBlaster II, USB-Blaster, or ByteBlasterMV cable with a 2.5- V VCCA supply. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a VCC power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the MasterBlaster Serial/USB Communications Cable User Guide.
7. Connect the series resistor at the near end of the serial configuration device.
8. These pins are dual-purpose I/O pins. The nCSO pin functions as FLASH_nCE pin in AP mode. The ASDO pin functions as DATA[1] pin in AP and FPP modes.
9. Resistor value can vary from 1 kΩ to 10 kΩ.
10. Only Cyclone IV GX devices have an option to select CLKUSR (40 MHz maximum) as the external clock source for DCLK.

**ISP of the Configuration Device**

In the second stage, the SFL design in the master device allows you to write the configuration data for the device chain into the serial configuration device with the Cyclone IV device JTAG interface. The JTAG interface sends the programming data for the serial configuration device to the Cyclone IV device first. The Cyclone IV device then uses the ASMI pins to send the data to the serial configuration device.