Design of the Front-End Readout Electronics for ATLAS Tile Calorimeter at the sLHC

F. Tang, *Member, IEEE*, K. Anderson, G. Drake, J.-F. Genat, *Member, IEEE*, M. Oreglia, J. Pilcher, and L. Price

***Abstract*—We present a detailed upgrade design of the analog front-end electronics for the ATLAS Tile Calorimeter (TileCal) at the sLHC. Here we use the latest commercial off-the-shelf (COTS) components. We believe that with the latest technology based COTS devices, significant improvements in radiation tolerance are possible. The front-end analog electronics provides 17-bit dynamic range for readout of the PMT signals. Each PMT signal is processed with a 7-pole passive LC shaper, followed by a pair of bi-gain amplifiers and two 40 Msps sampling ADCs. The readout system is capable of measuring energy deposition from ∼220 MeV to 1.3 TeV in a single calorimeter cell and providing input to a fully digital Level-1 trigger. Other on-board features include a slow current integrator used for detector calibration with a cesium source to normalize the PMT gains and charge injectors for calibrating linearity and dynamic range of the readout electronics. A total of ∼10, 000 upgraded readout channels are needed to replace the current system at the LHC.**

***Index Terms*—Analog-digital conversion, analog processing circuits, circuit noise, pulse measurements.**

I. Introduction

THE Atlas Tile Calorimeter (TileCal) is a cylindrical hadronic sampling detector with steel absorbers and scintillating plastic tiles, surrounding the EM calorimeter cryostat. It comprises a 6-meter-long central barrel detector (consisting of two 3-meter-long half barrels) ($|\eta| < 1.0$) and two 3-meter-long extended barrel detectors ($0.8 < |\eta| < 1.7$), each segmented azimuthally into 64 modules.

The corresponding detectors, i.e. TileCal cells, are 22 in each half central barrel and 16 in each extended barrel. The scintillating tiles are read out by wavelength shifting fibers that collect light from the cells to photomultiplier tubes (PMT). Each cell is read out from both sides independently, resulting in a total of ∼10, 000 readout channels. The details of the structure of the TileCal are given in [1]–[3].

II. Tile Calorimeter Analog Front-End Readout Requirements

Fig. 1 shows the Tile Calorimeter and its Electronics Drawers. A total of 256 Electronics Drawers are installed in the central and the extended barrels at the outer radius of the calorimeter. Each drawer can house maximum of 48 PMT blocks, the high voltage distribution and front-end readout electronics, as well as digitizers, optical data links and low voltage DC-DC converters etc. For the barrel modules, 44 PMTs blocks are required. The extended barrel drawers use 32 of the PMT positions.

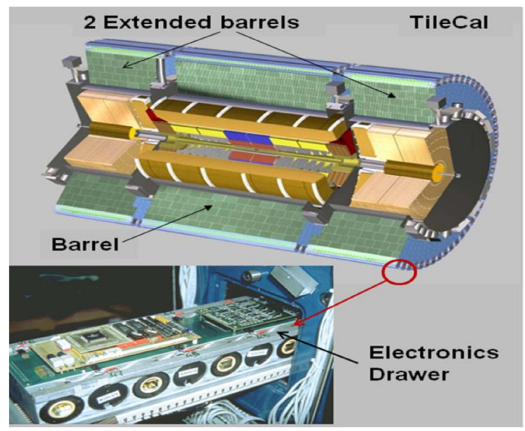

Fig. 1. Tile calorimeter and electronics drawers.

The luminosity of the sLHC is planned to run up to $5 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$. Since the entire readout electronics inside the Electronics Drawers are exposed to radiation while the experiment is running, the increased radiation levels and the limited component lifetime will eventually necessitate an upgraded design to replace all of the readout electronics [5]–[9] in the present TileCal.

The upgraded system design guideline will focus on following three aspects:

a) Designing a readout electronics system with the required electronics performance and with sufficient radiation hardness.
b) Providing input to a fully digital Level-1 trigger.
c) Reducing power consumptions and the number of the low voltage DC power supplies used in the readout system.

The above mentioned design guidelines should provide a less complicated, more reliable and better performing system for the sLHC.

However, based on the experience from physics conducted at ATLAS, detailed upgrade design specifications for the TileCal analog front-end electronics should include:

1) Implementing a readout system with 17-bit dynamic range. The ATLAS TileCal analog front-end electronics is required to measure the energy deposition in a single TileCal cell from 220 MeV to 1.3 TeV. The corresponding maximum PMT output charge is ∼800 pC. The 17-bit dynamic

Manuscript received June 14, 2010; revised October 28, 2010, February 11, 2011, and April 03, 2011; accepted April 07, 2011. Date of publication September 20, 2012; date of current version April 10, 2013.

F. Tang, K. Anderson, J.-F. Genat, M. Oreglia and J. Pilcher are with the Enrico Fermi Institute, The University of Chicago, Chicago, IL 60637 USA (e-mail: tang@edg.uchicago.edu).

G. Drake and L. Price are with Argonne National Laboratory, Lemont, IL 60439 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNS.2012.2215053

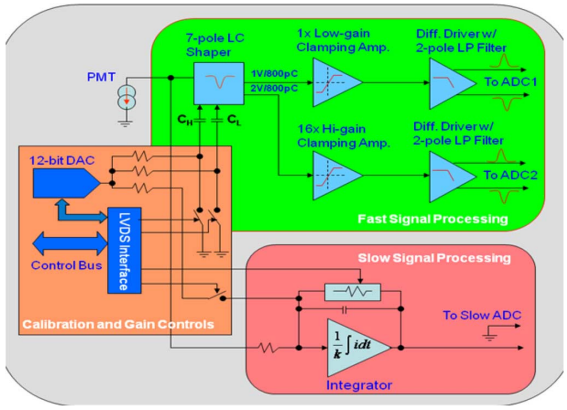

Fig. 2. Diagram of the analog front-end readout electronics.

range is achieved by using a high sensitivity shaper and a pair of bi-gain amplifiers with a total gain ratio of 32, along with two 40 Msps 12-bit sampling ADCs in parallel to process each PMT output signal. With this system, a particle that has a least energy deposition in a cell (e.g. a 220 MeV muon) will yield about 10 to 35 counts from a single PMT output. The energy deposition varies with the cell locations.

2) Being capable of precise electronic calibration of each readout channel. The electronic calibration is conducted by using two charge injectors which can cover the entire dynamic range. The calibrating system must present linearity better than 0.3% and amplitude accuracy better than 0.1%.
3) Being capable of monitoring the PMT minimum bias current during proton-proton collision and performing TileCal detector and PMT gain calibration. This is done by using a radioactive cesium sources that travels through a hole in the scintillating tiles of the calorimeter cells.

III. Front-End Analog Readout Electronics

The front-end analog electronics printed circuit board, which has a dimension of 7 cm × 4.7 cm, sits inside the PMT block in the TileCal [4]. Fig. 2 shows a diagram of the analog front-end readout electronics. The analog signal processing is divided into three parts: a fast signal processing chain, a slow signal processing chain (integrator), and an electronic calibration and control system.

A. The Fast Signal Processing Chain

The fast signal processing chain includes a 7-pole passive LC shaper, a pair of bi-gain clamping amplifiers, and a pair of differential drivers which feed low-gain and the high-gain signals to the digitizers that resides on the Main Board in the same Electronics Drawer.

With a channel gain ratio of 32 and dual channel 12-bit ADCs in parallel, the readout electronics achieves a dynamic range of 17-bits.

A simplified schematic of a 7-pole passive LC shaper is shown in Fig. 3. Charge injectors are included for electronic calibrations.

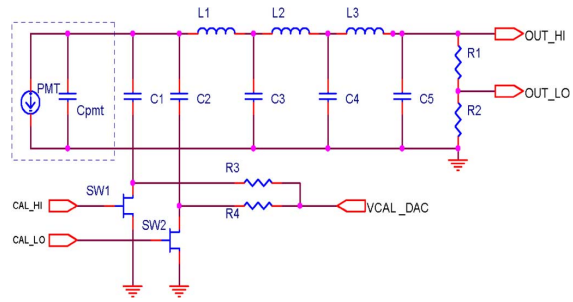

Fig. 3. Simplified schematic of a 7-pole passive LC shaper.

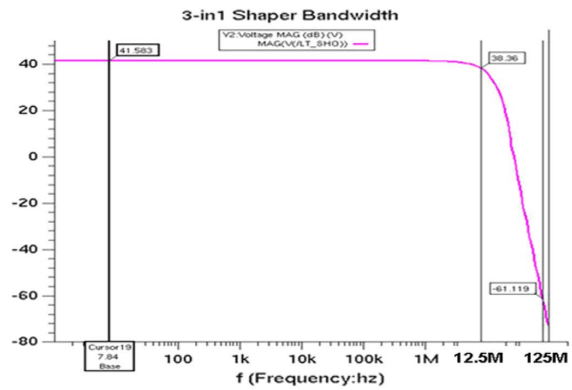

Fig. 4. 7-pole passive LC shaper bandwidth and its bandwidth roll-off.

The shaper was designed to achieve an optimal signal-to-noise ratio and to shape the PMT fast signal into a "slower" signal, whose pulse shape can meet the Nyquist criterion for the 40 Msps digitizer. It has a bandwidth of ∼12.5 MHz at −3 dB and with the effective bandwidth roll-off slightly greater than −100 dB per decade in the 1st Nyquist zone. In the 2nd Nyquist zone, where the bandwidth roll-off is −140 dB per decade, the noise mapped back from 2nd Nyquist zone can be ignored. The chart of the shaper bandwidth and bandwidth roll-off is shown in Fig. 4.

The shaper has an output impedance of 126 ohms, with two outputs which provide the sensitivity of 2 V/800 pC and 1 V/800 pC respectively. The transient response to a typical TileCal PMT pulse has a rise time of ∼5 ns and a pulse width of ∼18 ns full width at half maximum (FWHM). The shaper output is a very symmetrical unipolar pulse with a peaking time of 25 ns and a pulse width of 50 ns FWHM. Another advantage when using a passive LC shaper is that we can directly inject charge into the system using two capacitors in the first stage of the LC network. This allows high-gain and low-gain channel calibration without affecting the characteristics of the shaper. In Fig. 5, the transient response of the shaper to a typical 2 pC PMT pulse is shown.

The capacitors C1 and C2 are not only implemented as basic shaper components, but also serve as charge injectors. The electronic calibration of the high-gain channel is entered via C1 (6.2 pF) and SW1, while the calibration of the low-gain channel is entered via C2 (200 pF) and SW2. A 12-bit digital-to-analog converter (DAC) charges C1 or C2 to up to 4 V, Charging C1 allows the injection of a charge in the range 0–25 pC, which covers the dynamic range for the high-gain channel. Similarly,

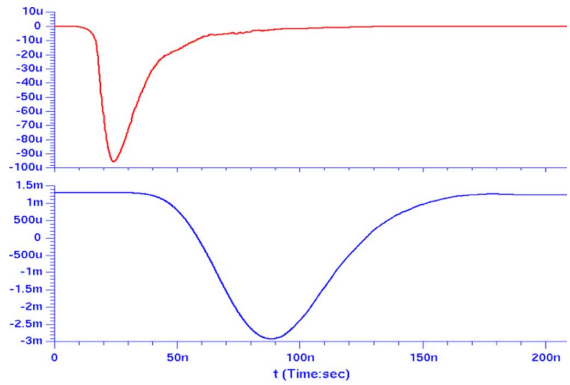

Fig. 5. Shaper transient response to a typical of 2 pC PMT pulse. The PMT output signal is shown at the top plot and the shaper output signal is shown at the bottom plot.

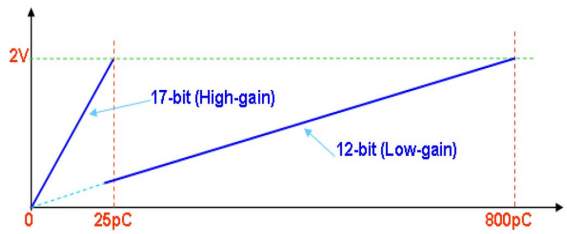

Fig. 6. Resolution of the bi-gain readout front-end electronics.

C2 allows injecting a charge between 0–800 pC, which covers the dynamic range of the low-gain channel.

The charge injector switches SW1 and SW2 are closed in normal run mode. For the high-gain channel calibration, only the SW1 is opened to allow C1 to be charged to a desired voltage. The charge $(Q = C1^{*}V)$ will be injected into the shaper in a transient time less than 1 ns on SW1 closing. Similarly, for the low-gain channel calibration, only SW2 is opened and closed. Since the on-resistance of the switches is less than 1 Ω, the charge injection time is less than 1 nS. Compared to the 25 nS shaping time of the shaper, the switch transient time and the switch on-resistance have small effects on the pulse shape and can thus be ignored.

Fig. 6 shows the resolution of the bi-gain readout system. As was mentioned above, the bi-gain channels have a gain ratio of 32 and are followed by two 12-bit ADCs in parallel. The readout system has a dynamic range to 17-bits. The high-gain channel will cover an effective signal dynamic range of 0–25 pC, and the low-gain channel will cover an effective signal dynamic range of ∼25–800 pC.

In Fig. 7, a simplified schematic of the bi-gain readout electronics for the fast signal processing is shown. For input signals above 25 pC, the high-gain amplifier runs into saturation. This requires a fast recovering clamping amplifier to prevent the high-gain amplifier from deep saturation. In order to guarantee a uniform pulse shape for the bi-gain outputs, both channels must have same closed-loop bandwidth. We use the low power, high speed, current-mode clamping amplifier HFA1135 in our design. Unlike the voltage-mode amplifier, the bandwidth of the current-mode amplifier is basically independent of the close-loop gain. This feature ensures that the low-gain amplifier U1 and hi-gain amplifier U2 have the same bandwidth although

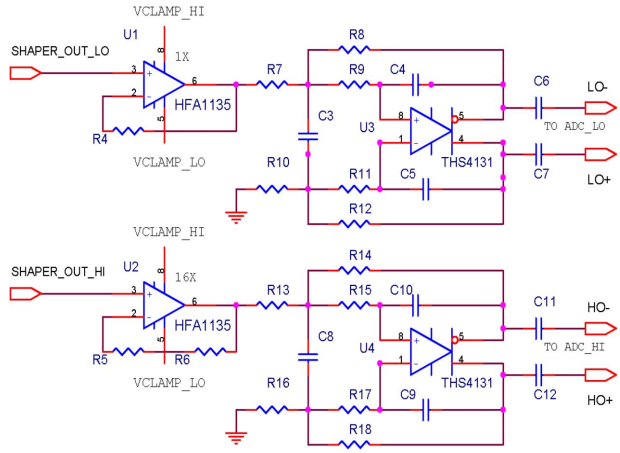

Fig. 7. Simplified clamping amplifiers and differential drivers with 2-pole active filter.

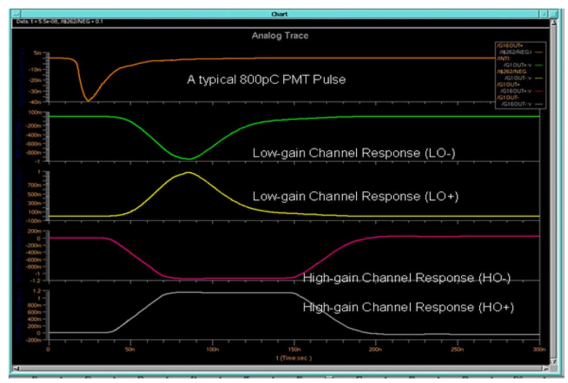

Fig. 8. Transient responses of the bi-gain channels to the largest PMT pulse of 800 pC.

they work with different closed-loop gains. HFA1135 has very fast overdrive recovery time on the order of a few nanoseconds. This functionality not only allows us to set the proper output voltage swings to protect downstream circuit from damage or input saturation, but also ensures a quick return to linear operation following an overdrive signal. Since the sLHC will produce collisions every 25 ns, HFA1135 should not cause any dead time because of overdrive. The full differential drivers U3 and U4 are configured as a 2-pole low-pass active filter with a bandwidth of ∼30 MHz. This will further help reduce the high frequency noise and boost the system signal-to-noise ratio without significantly affecting the pulse shape.

The transient response of the bi-gain channels to an 800 pC PMT pulse is shown in Fig. 8. With this large pulse input, the low-gain channel reaches a full scale differential swing of 2 V, while the high-gain channel outputs are well clamped and then recover in a few nanoseconds after the input signal ends.

With a fully digital implementation of the Level-1 trigger, raw data from each bi-gain readout circuits in an Electronics Drawer is sent to the off-detector readout modules (ROD), which are located 80 meters away.

We propose to use 4 identical Main Boards in each Electronics Drawer to digitize 48 PMT output signals and sending the data via optical links to the RODs. Each Main Board will digitize bi-gain outputs from 12 PMTs with 24 40 Msps ADCs

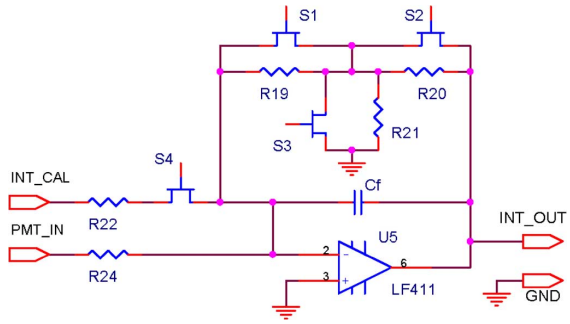

Fig. 9. Simplified current integrator and its electronic calibration circuit.

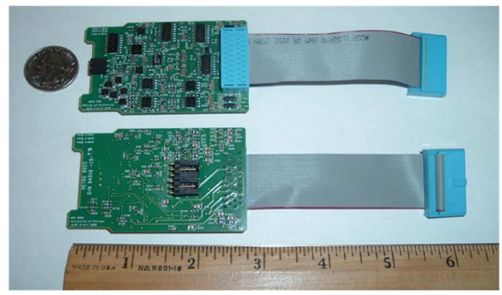

Fig. 10. A photo of the analog front-end card.

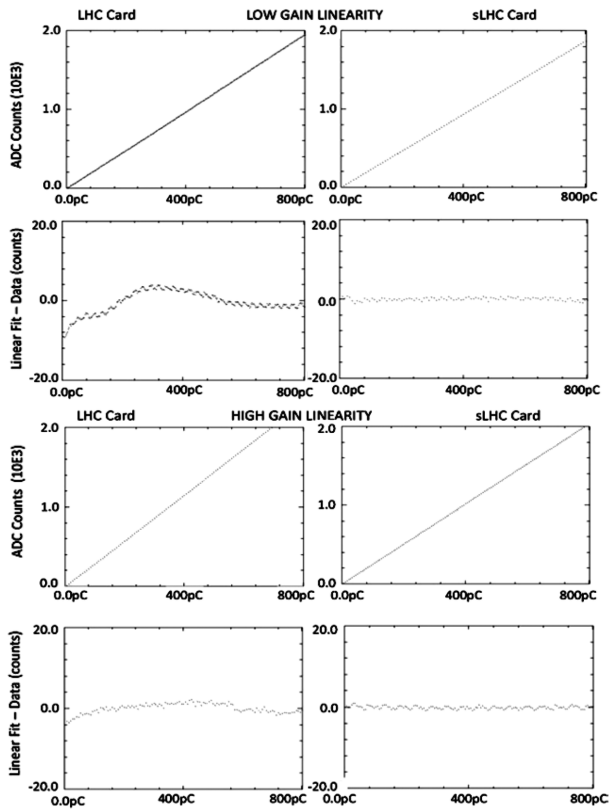

Fig. 11. Comparison of the linearity of the low-gain and high-gain channels between the LHC card and the sLHC card.

that working in parallel and synchronously. Without any protocol used, the raw data from bi-gain outputs of 12 PMTs would be 11.52 Gbps. The raw data from each Main Board will be packed into the GBT data format. This allows us to take advantage of the forward error correction which is implemented in the GBT protocol. The user data field of the GBT format is 80-bit wide. Therefore, 4 GBT data frames, corresponding to a total line rate of 19.2 Gbps, is the minimum required for each Main Board. With two times redundancy used in the data transmission, the total line rate per Main Board will be 38.4 Gbps. In addition, assuming that a single SNAP-12 module with 12 parallel optical fibers is used for the data transmissions from the Main Board to off detector RODs, a further 8B/10B encoding may be required. This increases the total line rate to 48 Gbps per Main Board, although each SNAP-12 fiber will only handle a line rate of 4 Gbps.

B. The Slow Signal Processing Chain

The slow signal processing chain includes a variable DC gain current integrator on the front-end board and a multiplexed 12-bit ADC for digitizing the integrator outputs on the Main Board. The integrator is designed to measure the PMT current induced by a radioactive cesium source as it traverses a hole through TileCal's scintillating tiles during detector calibration [6]. This calibration allows correction and normalization of the PMTs gains. The integrator will also be used to measure the PMT current induced by minimum bias proton-proton interaction at the sLHC. Since the minimum bias current in the calorimeter varies with the locations of the cells, the integrator has a variable sensitivity or variable DC gains. A simplified schematic of the integrator is shown in Fig. 9. The transimpedance of the integrator is set by a programmable resistor T-network controlled by S1, S2 and S3 for the three gain settings 7.5 MΩ, 20 MΩ and 54.3 MΩ, respectively. The time constant of the integrator is required to be greater than 10 ms, which gives a ripple less than 1 LSB of 12-bit ADC. The linearity with any gain settings should be better than 0.3% [1]. The S4 enables electronic calibration for the integrator. The calibration current is produced by a voltage source from an on-board DAC through a precision resistor R22.

C. The Electronic Calibration and Control Bus Interface

All of on-board electronic calibrations switch states, DAC value, and the integrator gains are controlled by LVDS bus lines that are connected to the Main Board through a 3-inch long 40-wire ribbon cable. The switch states, DAC value, and the integrator gain settings can be read back and monitored by the slow control processors.

IV. Test Results

The prototype analog front-end card was built and tested. In Fig. 10, a photo of the newly designed analog front-end readout card for the sLHC is shown.

The linearity and noise test results are shown in Fig. 11 and Fig. 12. Compared with the 3-in-1 front-end card (LHC Card) that is currently used at LHC, the newly designed TileCal analog front-end card (sLHC Card) for the sLHC gives better linearity and lower noise level ($<$1 LSB of 12-bit in the high-gain channel).

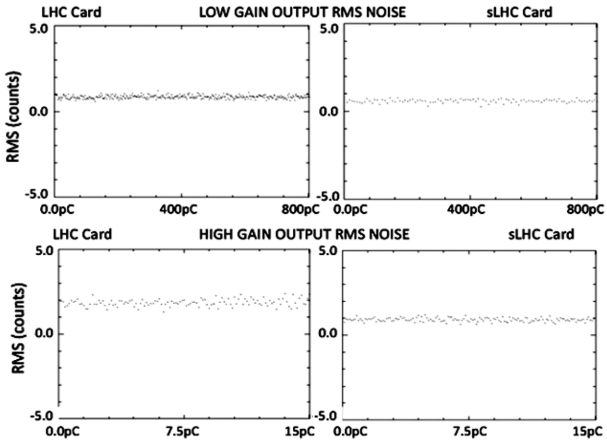

Fig. 12. Comparison of the output noise from the low-gain and high-gain channels between LHC card and sLHC card.

V. Conclusions and the Future Plans

Compared to the test results from the currently used 3-in-1 front-end readout card, the newly designed front-end card for the sLHC upgrade offers significantly improved electronics performance. Tests of radiation hardness are planned for the first half of 2010.

The TileCal front-end electronics will be housed inside the detector where the radiation level moderate. The electronics is required to survive testing to ∼60 Krad. If the COTS components based front-end electronics fails in the radiation test, the next design will concentrate on rad-hard, low power, high performance ASICs. The ASIC readout system will be most likely being designed with a similar scheme as was used with the COTS components. The detailed ASIC design will not be discussed in this paper.

References

[1] K. Anderson *et al.*, "Design of the front-end analog electronics for the ATLAS tile Calorimeter," *Nucl. Instr. Meth.*, vol. A 494, p. 381, 2002.

[2] The ATLAS TileCal Collaboration, Tile Calorimeter Technical Design Report 1996, *ATLAS Internal Note*, CERN/LHCC/96-42.

[3] F. Ariztizabal *et al.*, "Construction of performance of an ion-scientillator hadron calorimeter with longitudinal tile configuration," *Nucl. Instr. Meth.*, vol. A 349, p. 384, 1994.

[4] W. Smith, "Physics and detectors at the LHC and the sLHC," in *Proc. Conf. Record, ALCPG & ILC Workshop*, Snowmass, USA, 2005.

[5] K. Anderson *et al.*, "Design of the front-end analog electronics for the ATLAS tile Calorimeter," *Nucl. Instr. and Meth.*, vol. A 494, p. 381, 2002.

[6] Z. Ajaltouni, The Drawer System Concept for the ATLAS TileCal Readout *ATLAS Internal Note*, TileCal-NO-43, Dec. 1994.

[7] K. Anderson *et al.*, "Front end electronics for the ATLAS tile calorimeter," in *Proc. 4th Workshop Electron. LHC Experiments*, Rome, Italy, Sep. 21–25, 1998, pp. 239–245, LEB 98.

[8] S. Berglund *et al.*, "The ATLAS tile calorimeter digitizer," in *Proc. 5th Workshop Electron. LHC Experiments*, Snowmass, CO, Sep. 20, 1999.

[9] E. Starchenko *et al.*, "Redioactive source control and electronics for the ATLAS tile calorimeter cesium calibration system," *Nucl. Instr. Meth.*, vol. A 494, p. 381, 2002.

[10] K. Anderson *et al.*, "ATLAS tile calorimeter interface," in *Proc. 8th Workshop Electron. LHC Experiments*, Colmar, France, Sep. 9–13, 2002, pp. 269–273.