Design of Main Board for ATLAS TileCal Demonstrator

F. Tang, H. Akerstedt, K. Anderson, C. Bohm, K. Hildebrand, S. Muschter and M. Oreglia on behalf of the ATLAS Tile Calorimeter Group

Abstract— **The TileCal Demonstrator is a prototype for a future upgrade to the ATLAS hadron calorimeter when the Large Hadron Collider increases its luminosity in year 2023 (HL-LHC). It will be used for functionality and performance tests. The Demonstrator has 48 channels of upgraded readout and digitizing electronics and a new digital trigger capability, but stays backwards compatible with the present detector system by providing analog trigger signals. The Demonstrator is comprised of 4 identical "mini-drawers", each equipped with up to 12 photomultipliers (PMTs). The on-detector electronics includes 45 Front-End Boards, each serving an individual PMT; 4 Main Boards, each to control and digitize the 12 PMT signals, and 4 corresponding high-speed Daughter Boards serving as data hubs between on-detector and off-detector electronics. The Demonstrator is fully compatible with the present system, accepting ATLAS triggers, timing and slow control commands for the data acquisition, detector control, and detector operation monitoring. We plan to insert one fully functional Demonstrator module into the present ATLAS TileCal detector for the LHC RUN 2 in August 2014.**

This paper will only cover the design of the Main Board.

Index Terms—**Analog processing circuits, Circuit noise, Pulse measurements, Analog-digital conversion, Tile Calorimeter.**

I. INTRODUCTION

THE ATLAS Tile Calorimeter (TileCal) is a cylindrical hadronic sampling detector with steel absorbers and scintillating plastic tiles, surrounding the EM calorimeter cryostat. It consists of a 6-meter-long central barrel (i.e. two 3-meter-long half barrels) covering the rapidity range $|\eta| < 1.0$, and two 3-meter-long "extended barrel" detectors covering $0.8 < |\eta| < 1.7$. Each barrel is segmented azimuthally into 64 modules. The on-detector electronics of each barrel segment is housed in mechanical "superdrawers"[1], [2]. The entire TileCal has installed a total of 256 electronics drawers containing 9852 channels of on-detector readout electronics and corresponding high voltage and low voltage supplies.

The LHC Phase II Upgrade aims to increase the LHC luminosity by a factor of 10. This will lead to higher data rates requiring a more intelligent trigger, and will increase the ambient radiation seen by the electronics. The current analog

trigger system will be replaced by a fully digital Level-1 trigger. A Demonstrator superdrawer is being developed to cover one slice of detector with 45 photomultipliers. It will help to understand the readout electronics and to gain field experience with the final Phase II upgrade design. In order to build a fully functional digital trigger and readout system for evaluation and making them compatible with the present analog trigger scheme, the Demonstrator electronics must be equipped for both analog and digital triggering.

II. TILECAL DEMONSTRATOR READOUT ELECTRONICS

In LHC Run 1 the maximum instantaneous luminosity achieved was 8×10^{33} cm^{-2}s^{-1}. For Run-2 in 2015, the luminosity of the LHC will increase to $5 \sim 7 \times 10^{34}$ cm^{-2}s^{-1} [3]. Since the readout electronics inside the Electronics Drawers are exposed to radiation while the experiment is running, the increased radiation levels and the limited component lifetime for current electronics will eventually necessitate an upgraded design to replace all of the readout electronics in the present TileCal. [4]-[6].

Since the 2023 upgrade will require a complete redesign of all on- and off-detector electronics so will the Demonstrator and all its systems components, including drawer mechanics, data digitization and off-detector data acquisition electronics, Level-1 trigger, high voltage supply distribution and PMT base, low voltage supplies, as well as detector control and calibration systems.

The Demonstrator on-detector electronics consists of 45 Front-End Boards (FEB: amplifier/shaper/calibration), 4 Main Boards (MB: LV/signal routing/digitization/control), and 4 Daughter Boards (DB: serialization/communication). Each MB+DB is an independent system communicating off-detector via high speed optical fibers. The system is mounted in a water-cooled "minidrawer", 4 of which are mechanically connected to form a complete barrel superdrawer. All communication to the off-detector readout module (sROD) is handled by the DB, apart from the analog trigger signals required for backward compatibility. This communication includes detector data, timing and slow control (TTC) commands for digitizer synchronization, and configuration of the readout electronics, such as charge injection calibration for the on-detector electronics and Cesium source calibration for the detector and PMTs [7]. However, the Cesium signals are read out separately by integrating the PMT current.

III.   DESIGN OF MAIN BOARD

At present, the digitized data is stored in pipeline buffers on a digitizer board and only read out if the event is accepted by the Level-1 trigger based on analog sums of Tile towers [8], [9]. The HL-LHC will require more sophisticated algorithms based on more detailed information. All raw data from each PMT are directly sent to the off-detector electronics for further trigger processing and data acquisition. To cover the required dynamic range they are sent in two versions, high gain and low gain. Each Demonstrator MB contains data digitizers for 12 PMTs, for low gain and for high gain signals.

The phase of the sampling clocks can be adjusted by FPGAs on the MB to compensate the analog signal delays due to different path lengths from the PMTs. Each FPGA on the MB will directly communicate with the DB via its dedicated SPI interface.

The Demonstrator's MB contains commercially available off-the-shelf components. Each bi-gain fast signal pair is digitized in parallel by a dual 12-bit 40 Msps ADC (LTC2264-12). The two channels are sent out to the DB via a two-bit serial bus at a speed of 560 Mbps (14 bit x 40 Msps). Each data word is aligned by a data clock (280MHz) and a data frame clock (40MHz). The ADC has an analog input dynamic range of 1V peak to peak. For achieving a proper DC bias for input dynamic range, adjusting the baseline shift caused by the capacitive coupling, each ADC channel includes two 12-bit DACs, which allow control of the dynamic range.

The integrator output of each analog Front End Board is digitized by a 50 kHz 16-bit ADC, readout by an I^{2}C bus. A readout rate of a few kHz will be sufficient. The diagram of one channel of PMT data flow on the MB is shown in Fig. 1.
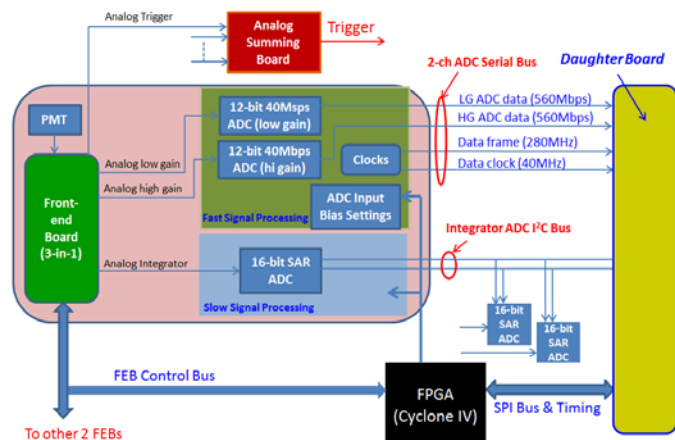

Fig.1. Diagram of a single PMT readout channel

In order to reduce data latency and minimize the effect of single even upsets in the FPGA due to ambient radiation, all the ADC output data will be directly sent to DB without buffering in the FPGAs on the MB, which also results in lower trigger latency.

Fig. 2 shows the first prototype of the MB. It measures 690 mm by 100 mm. In order to reduce the possible failures caused by low voltage supply trips, the MB layout is physically divided as two regions. Functionally, the two regions are operating independently.

Fig. 2. Main Board for the Demonstrator.

Each region of a MB takes its own single +10V input supply from the patch panel of the drawer and regulates it down to the 9 different low voltages used by the FEB, MB and DB electronics. The on-board diode-OR circuit for two +10V input supplies provide redundancy for the on-detector electronics; if one +10V feed fails, the other +10V supply will automatically take over. All local low voltage values for the on-detector electronics can be continuously monitored by the DB with embedded ADCs in the Kintex 7 FPGAs.

The Tile barrel steel provides good radiation shielding, except at the exposed "near" ends where the LV power bricks are located. To enhance the radiation tolerance, the point of load regulators are all laid out in the far-end of the MB, where the radiation is significantly reduced. All the regulator chips have thermal sinks mounted on the back side of the printed circuit board (PCB), where we can attach thermal pads conducting the heat from the devices directly to the water cooled drawer frame.

The PCB layout of the MB is very challenging since it is a very long and narrow board with mixed signals. Less than 1 count rms noise can be tolerated in the 12-bit ADCs, and the 24 channels of digitized data are required to transmit at a speed of 560 Mbps to a 400-pin interconnector interface to the DB. In addition, there are more than 10 channels of DC/DC switchers mounted on the board, which generate switching noise on the board. A good local isolation between analog and digital signals return paths is crucial to stop ground bounce. Therefore, careful consideration was given to the layout of the MB to preserve the analog and digital signal integrity. Switching phases of the DC/DC switchers were balanced to minimize the switching noise. The PCB is laid out in 6 signal layers and 8 power layers, and 3 redundant non-split ground layers are used for improving the signal integrity of the fast analog and digital signals.

IV.   THE TILECAL DEMONSTRATOR TEST SETUP

MB tests started in fall 2013. The firmware of the MB is currently under test. Both DB and sROD will be available for system tests in June 2014.

V.   SUMMARY

In order to study the design a new readout and data acquisition system for the Phase II TileCal upgrade, a Demonstrator has been built with completely re-designed electronics and mechanics. This Demonstrator will be used to perform functionality and performance tests when inserted into the TileCal detector in August 2014. The readout and digitizing system employ commercially available off-the-shelf, advanced deep-micron components. The system has 17-bit

linear dynamic range with a good signal-to-noise ratio for the readout of PMT signals. It is capable of forming both analog and fully digital L1Calo triggers simultaneously. The goal of building a Demonstrator is to understand the design challenges in the future Phase II upgrade and to gain field experience, including experience with the design of low noise readout front-end electronics, very high speed data transmission, precise and low jitter timing implementations, as well as digital triggering algorithm evaluations.

VI.   ACKNOWLEDGEMENT

REFERENCES

[1] The ATLAS TileCal Collaboration, "Tile Calorimeter Technical Design Report," *ATLAS Internal Note*, CERN/LHCC/96-42, 1996.

[2] Z. Ajaltouni, et al., "The Drawer system concept for the ATLAS TileCal readout," *ATLAS Internal Note*, TileCal-NO-43, December 1994.

[3] M. Oreglia on behalf of the ATLAS Tilecal Group. Upgrading the ATLAS Tile Calorimeter Electronics. ATL-TILECAL-PROC-2013-009

[4] K. Anderson et al., "Design of the front-end analog electronics for the ATLAS tile Calorimeter," *Nucl. Instr. and Meth.*, A 494 (2002) 381.

[5] F. Ariztizabal, et al., "Construction of performance of an Iron-scientillator hadron calorimeter with longitudinal tile configuration," *Nucl. Instr. and Meth.,* A 349 (1994) 384.

[6] W. Smith, " Physics and detectors at the LHC and the sLHC," *Conf. Record,* ALCPG & ILC Workshop, Snowmass, USA, 2005.

[7] E. Starchenko, et al., "Redioactive source control and electronics for the ATLAS tile calorimeter cesium calibration system,"
Nucl. Instr. and Meth., A 494 (2002) 381

[8] S. Berglund, et al., "The ATLAS tile calorimeter digitizer," *Proceedings of 5th workshop on electronics for LHC experiments,* Snowmass, Colorado, 20 September 1999.

[9] C. Bohm on behalf of the ATLAS Tile Calorimeter System. "A Hybrid Readout System for the ATLAS TileCal Phase 2 Upgrade Demonstrator". ATL-TILECAL-PROC-2012-014.