Upgrade Analog Readout and Digitizing System for ATLAS TileCal Demonstrator

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***Abstract*— A potential upgrade for the front-end electronics, signal digitization, and data acquisition system of the ATLAS central hadron calorimeter for the High Luminosity Large Hadron Collider (HL-LHC) is described. A Demonstrator is being built to readout a slice of the TileCal detector with this system. The on-detector electronics includes up to 48 analog Front-end Boards for processing the PMT signals, 4 Main Boards for data digitization and slow controls, 4 Daughter Boards with high speed optical links to interface the on-detector and off-detector electronics. Two new ReadOut Driver Boards are used for off-detector data acquisition and preprocessing the digital trigger signals.**

The ATLAS Tile Calorimeter on-detector electronics is placed in "drawers" at the back of each of 256 detector wedges. Each drawer services up to 48 photomultiplier tubes. The new readout system is designed to replace the present system as it will exceed component lifetime and radiation tolerance limits making it incompatible with continued use into the HL-LHC era.

With the Demonstrator, we are preparing test samples of each of the components needed for the full upgrade. It is envisioned that one drawer of the new electronics will be installed in the detector for the LHC RUN 2 in 2014. For compatibility the system will maintain the current analog trigger and will permit us to acquire experience and to study in detail a fully digital trigger scheme without compromising the present trigger system.

***Index Terms*—analog signals processing, electronics noise, shaper, waveform sampling, digital trigger, Tile Calorimeter.**

I. Introduction

THE ATLAS Tile Calorimeter (TileCal) is a cylindrical hadronic sampling detector with steel absorbers and scintillating plastic tiles, surrounding the EM calorimeter cryostat. It comprises a 6-meter-long central barrel detector (consisting of two 3-meter-long half barrels) ($|\eta| < 1.0$) and two 3-meter-long extended barrel detectors ($0.8 < |\eta| < 1.7$), each segmented azimuthally into 64 modules. The 6-meter-long module in the central barrel contains two electronics "drawers" (see Fig 1) while each module in extended barrels contains only one [1], [2]. TileCal has installed a total of 256 electronics drawers containing ~10,000 channels of on-detector readout electronics and the corresponding high voltage and low voltage power supplies.

The TileCal Phase II Upgrade project is a complete re-design of the readout electronics and data acquisition system scheduled to occur between 2022 and 2024. It must process TileCal data with the averaged LHC luminosity increased by a factor of ~10. The current analog trigger system will be replaced by a fully digital trigger with access to all the TileCal data rather than a reduced set where TileCal cells have been summed into trigger towers as is done in the present design. A demonstrator is being developed to evaluate the new readout electronics performance and gain field experience for the Phase II upgrade design. In spite of the fully functional digital trigger, the Demonstrator must also provide an analog trigger to make it compatible with the present analog trigger scheme. The Demonstrator is planned to be inserted into the TileCal for LHC RUN 2 in 2014.

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II. TileCal Demonstrator Readout Electronics

By LHC Run 1, the luminosity reached $8x10^{33}$ $cm^{-2}s^{-1}$. In 2022, the luminosity of the HL-LHC is planned to increase to $5\sim7x10^{34}$ $cm^{-2}s^{-1}$ [3]. Since the on-detector readout electronics is exposed to activating radiation while the experiment is running, the increased radiation levels and the limited component lifetime will eventually necessitate an upgrade to replace all of the readout electronics in the TileCal. [4]-[6].

The present TileCal electronics is placed in "drawers" as shown in Fig. 1. It contains 9 different functional boards which are stacked in 4 levels inside the drawer.

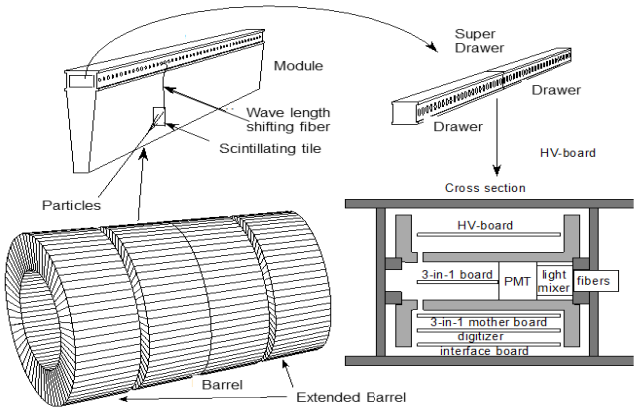

Fig. 1. Tile calorimeter and electronics drawers

Although the Demonstrator will replace only one electronics drawer, an extensive series of tasks must be undertaken before this new drawer can be deployed. These

tasks include a re-design of the drawer mechanics with active water cooling. The analog front-end has been redesigned. A new data digitizing scheme, slow control and timing synchronization, parallel analog and digital trigger schemes, high voltage control and distribution, new higher current PMT high voltage divider, low voltage supplies, detector testing-calibration bench and the off-detector readout driver all must be implemented. The experience we will gain from this work will help us to address the system issues and solve the problems that we may encounter in the future Phase-II TileCal upgrade.

Instead of 9 types of boards used in the present TileCal readout system, the Demonstrator electronics is built with only 4 types of functional boards: Analog Front-end Board, Main Board, Daughter Board and High Voltage Distribution Board. Fig. 2 shows a diagram of the Demonstrator readout electronics mounted on one drawer. The Analog Front-end Board resides in the PMT enclosure (block); the shaped and amplified analog signals are feed to the Main Board for data digitization.

The newly designed electronics drawer is composed of 4 identical mini-drawers with water cooling connected inside the supporting frames. Each mini-drawer will mount up to 12 PMT blocks, one Main Board and one Daughter Board. The Demonstrator retains all the functionalities of the present readout system, and adds the capabilities of a fully digital triggering.

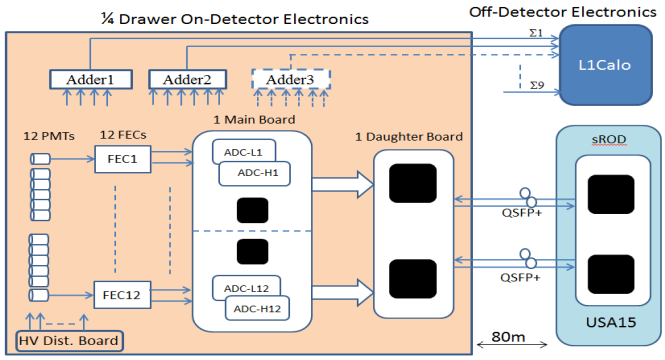

Fig. 2. A diagram of the readout electronics in a mini-drawer (1/4 drawer).

A. Analog Front-end Readout Board

The ATLAS TileCal analog front-end electronics is required to measure the energy deposition in a single TileCal cell from 220MeV to 1.3TeV. The corresponding maximum PMT output charge is ~800pC. Three types of analog front-end boards with different readout methods are being developed by three institutions.

The analog front-end electronics Option-I is based on the present so-called 3-in-1 card. It consists of a passive 7-pole LC shaper with two clamping amplifiers for fast signal processing, a slow integrator for minimum bias monitoring and a Cs137 source calibration of the PMT gains. The high gain and low gain amplifiers have a gain ratio of 32; each followed by a 12-bit 40Msps ADC, covering a dynamic range of 17 bits [8], [9]. This board is developed by the University of Chicago.

The analog front-end electronics Option-II under development by Laboratoire de Physique Corpusculaire de Clermont-Ferrand (LPC), France, is designed as an ASIC chip, called FATALIC. The chip is working as a current conveyor, where a PMT current signal is copied to three outputs in different current gains (1x, 8x and 64x), and each output will be followed by an external 12-bit sampling ADC to cover a dynamic range of 17 bits.

The analog front-end electronics Option-III is based on a modified Charge Integrator and Encoder (QIE) chip, developed by Fermilab and Argonne National Laboratory. A QIE chip divides the input signal into 4 ranges, with each range integrating a scaled fraction of the current signal into ranges with the current maxima: 16i/23, 4i/23, 2i/23 and i/23, respectively. Each range has a gated integrator and a 6-bit flash ADC. The four ranges cover a dynamic range of 17 bits, but each range gives 8-bit resolution.

Fig. 3 shows a photograph of the Option-I analog front-end board adopted in the Demonstrator for LHC RUN 2 as it is the only Front-End that can deliver an analog trigger signal. The board, sized 70mm x 47mm, sit inside a PMT block in the TileCal detector. A 40-conductor control bus is implemented mainly for front-end electronics configuration and controls. All control bus signals are operated in LVDS. A pair of high gain and low gain analog signal cables bring the differential signals to the Main Board for data digitization and another analog cable sends the analog differential signal to the Summing Card for transport to the analog trigger.

Fig. 3. A photograph of the Analog Front-end Board

A diagram of the upgraded analog front-end readout electronics for the Demonstrator is shown in Fig. 4. The PMT analog signal is processed in real time along two paths: the fast and the slow signal processing chains.

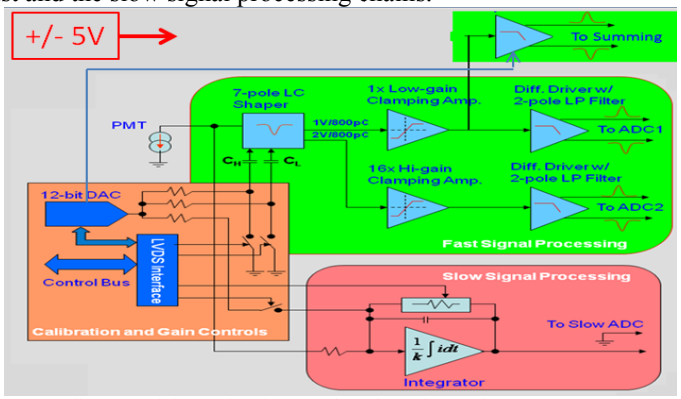

Fig. 4. A diagram of the analog front-end readout electronics.

The fast signal processing chain includes a 7-pole LC shaper and two parallel clamping amplifiers with a gain ratio of 32. Each analog signal is digitized by a 12-bit 40Msps ADC. 17-bit dynamic range is achieved. With this system, a particle that has a least energy deposition in a cell (e.g. a 220MeV muon

particle) will yield about 10 to 35 counts from a single PMT output with a good signal noise ratio (rms noise of 1-2counts).

The shaper has a sensitivity of 2V/800pC and a shaping time of 25ns with approximately symmetrical rising and falling times at the output. The output pulse width is ~51ns FWHM and the output impedance is 126Ω. With the gain ratio of 32, the high gain channel has a dynamic range of 0 to 25pC, while low gain channel has a dynamic range of 0 to 800pC.

The slow signal processing chain includes a slow integrator that is designed to monitor the minimum bias current of the PMTs during proton-to-proton collisions; and evaluate the long term detector efficiency and the PMT stability. Since the minimum bias current varies from location to location in the detector, the integrator needs to measure the bias current in a range from 2nA to 4uA, thus, 6 programmable transimpedance values of 2.7MΩ, 25MΩ, 27.MΩ, 52.7MΩ, 72.7MΩ and 97.MΩ can be set to adjust the integrator sensitivity. The integrator is able to achieve <1% energy resolution over the entire dynamic range.

The other tasks of the integrator are to check the light path from each scintillating tile to its PMT and to calibrate the TileCal detector and the PMT gains. By checking the light path and light intensity measurement, defective detector tiles or bad fiber connections inside detector cells can be found. This task is done by using a Cs137 source that travels through holes in the scintillating tiles of the calorimeter cells while the current from the integrator [7] is being read out. The integrator output is sent to the Main Board for digitization via two wires in the control bus.

An on-board charge injection calibration system, with linearity better than 0.3% and amplitude accuracy better than 0.1% over the entire dynamic range of 0-800pC is implemented for fast electronics calibration. This calibration is used to normalize the channel gains and gain ratio between high gain and low gain channels, as well as to examine system linearity and noise. The charge injection can also be used to analyze trigger algorithms by injecting charges to a number of specific channels in one or more trigger towers to emulate the particle tracks. The other on-board electronics calibration implementation is to calibrate the integrator gains and evaluate the integrator output ripple, noise and pedestal. These features make system performance and triggering algorithm tests feasible and efficient.

In addition, to comply with the present analog trigger system and compare the analog and digital trigger mechanisms in real time, an analog trigger output still is retained in the analog front-end board. In the Phase II upgrade, the analog triggering will be completely removed since then the fully digital trigger scheme will be the default.

B. Main Board

In the present TileCal readout system, the digitized data are stored in pipeline buffers on digitizer board and only read out if the events are accepted by the first level trigger. The trigger signals are generated by analog summation of the PMT signals into trigger tower sums [10], [11]. The HL-LHC will produce more complex events that will require more competent algorithms in more detailed information to bring down the rates to acceptable levels. Thus, the Main Board design will aim at a fully digital trigger scheme, where all of the digitized data will be directly transmitted to the off-detector electronics.

The Main Board has 24 channels of 12-bit 40Mbps digitizers supporting 12 PMTs with bi-gain channel readout. For the other 12 channels 16-bit, 58.6kHz SAR ADCs are used for slow integrator readout. Because the time-of-flight, arrival time of signal detected by PMTs varies for different locations, the corresponding sampling clock phases of ADCs have to be adjustable to compensate the signal delays. For above reasons, the Main Board divides the 12 PMTs into be 4 groups; where each group employs a low cost FPGA (Altera Cyclone IV) that serves as control and timing unit to configure three Analog Front-end Boards, as well as master the sampling clock phase for their ADCs. The FPGAs on the Main Board will directly communicate with the Daughter Board via their dedicated SPI bus to execute configuration commands.

The Main Board design is based on commercially available off-the-shelf components, and with qualified rad-hard requirements. The dual 12-bit 40Msps ADC chip (LTC2264-12) is used to digitize the PMT signals from the bi-gain channels; it uses a single 1.8V supply, consuming 56mW per channel. A serial data bus is implemented to send data at a rate of 560Mbps (14-bit x 40Msps in the default mode) to the Daughter Board. The ADC also generates a 280MHz data latching clock and a 40MHz data frame clock for data alignment. The data is latched at the clock rising and falling edge. The ADC analog input dynamic range is 0-1V peak to peak with a common mode voltage of 0.9V. The proper DC biases at the ADC differential inputs are required for a level shifter, which translates the back-to-back differential signal (one side swings from 0 to positive, the other side swings from 0 to negative) to true differential signals with a common mode voltage of 0.9V. The bias voltages can be set individually by a multi-channel 12-bit DAC (LTC2656).

Since the integrator output is slow, each output can be digitized by a 16-bit, 58.6kHz ADC (Max1169), and every 3 integrator ADCs share an I^2C bus to send data to the Daughter Board. A readout rate of the integrator ADC from a few tens of Hertz to a few hundred Hertz will be sufficient; the oversampled data can be further averaged in off-detector electronics for suppressing the noise.

A diagram of a single PMT readout flow on the Main Board is shown in Fig. 5.

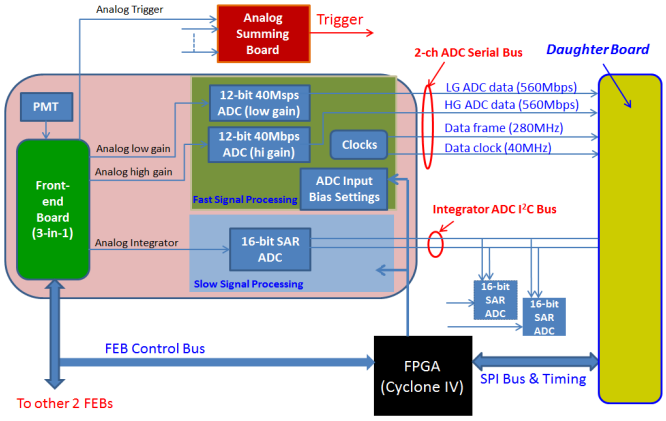

Fig. 5. A diagram of a single PMT readout.

In order to reduce data latency and minimize the effects of single event upset in the FPGAs due to the radiation environment, the ADC output data will be directly routed to the Daughter Board without buffering in an FPGA on the Main Board. The low latency readout scheme will benefit the digital triggering in real time.

Fig. 6 shows the first prototype of the Main Board. It is sized 690mm x 100mm. To increase system reliability, an on-board diode-OR circuitry is added for power supply redundancy. The layout of the Main Board is physically divided into two sections; each with its own single +10V power supply input via the patch panel. In the case of normal operation, the diode-OR is turned off, so that the two sections work independently. However, if the power supply in one section fails, the diode-OR will turn on, and the other supply will automatically take over and supply both sections.

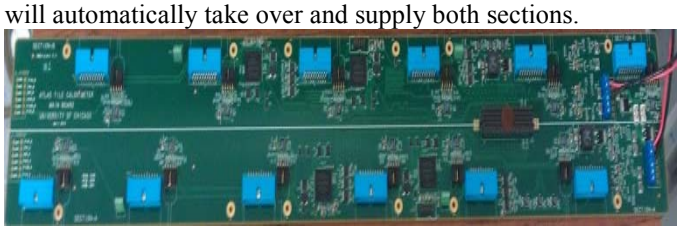

Fig. 6. A photograph of the first prototype of the Main Board.

The highest radiation levels the electronics will encounter is for the electronics mounted near the gap between the barrel and extended barrel modules. The radiation drops off rapidly as the distance from the gap increases and is reduced by a factor of 10 halfway down the length of the Main Boards. For this reason, the Point Of Load regulators and other critical components are all laid out at the far-end, where the radiation exposure is lower. All the regulator chips requiring thermal sinks are mounted on the back side of the printed circuit board (PCB), the thermal pads or thermal couplers conduct the heat from the devices directly to the water cooled drawer frame.

The Main Board PCB layout is very challenging since very fast digital signals and very low noise analog signals are routed in a limited space. The board has 24 channels of analog electronics being placed at specific locations to ensure the analog performance. Each ADC transmits the data at a rate of 560Mbps to the Daughter Board via a FMC 400-pin connector at the far-end. The longest traces at such high speed are more than 20 inches, and the fact that they cross a few analog blocks, makes it very difficult to achieve noise immunization.

In total, more than 10 channels of on-board DC/DC switching regulators have been mounted on the far-end of the board due to radiation concerns. The DC/DC switching regulators generates 5 primary local voltages (+5V, -5V, +2.5V, +1.8V, +1.2V) which are filtered before reaching 9 different analog and digital loads in each section. DC/DC switching regulators are the major noise sources on the board. Therefore, a good local isolation and signal integrity for the analog and digital signals return paths are very crucial to reduce ground bounce, crosstalk and noise pickup. Designing balanced switching phases of the DC/DC switchers will also help minimize electromagnetic interference.

The PCB is laid out in 6 signal layers and 8 power layers, where 3 redundant non-split ground layers are used for improving signal integrity and minimize the signal crosstalk.

C. Daughter Board

The Daughter Board, developed at Stockholm University, is a data hub responsible for the multi gigabit data communication between on-detector and the off-detector, as well as for controlling and monitoring all the on-detector electronics [12], [13]. To reach the Demonstrator goal, the hardware and firmware have to be thoroughly tested, verified and later proven to be sufficiently radiation tolerant. Although a first generation of the Daughter Board addressed some of the issues, much remains to be studied with a second prototype. The hardware features of the second generation of the Daughter Board have now been tested and verified, including the electrical characterization of the gigabit transceiver performance at 10Gbps as well as user IOs at ~600Mbps for single data rate. The firmware was adapted to the upgraded hardware of the second generation Daughter Board, which includes a Kintex 7 FPGA and a 40Gbps QSFP+ module and an optional 60Gbps Avago Technologies' PPOD module (AFBR-775BEPZ) for high speed communication. Furthermore the clock layout was revised allowing reception of a 4.8Gbps data stream encoded with the CERN GBT protocol and transmitting data with either 5Gbps or 10Gbps which can be received without losing synchronization. Using this communication framework, on-board loopback tests with different setups were performed using two different custom evaluation boards. As a result the second generation Daughter Board is a major step towards a working Demonstrator. At this point most of the functionality of the second prototype has been verified and the process of manufacturing a final functional prototype has already started. The Daughter Board has been designed for redundant data transmission. The second generation prototype of Daughter Board is shown in Fig. 7.

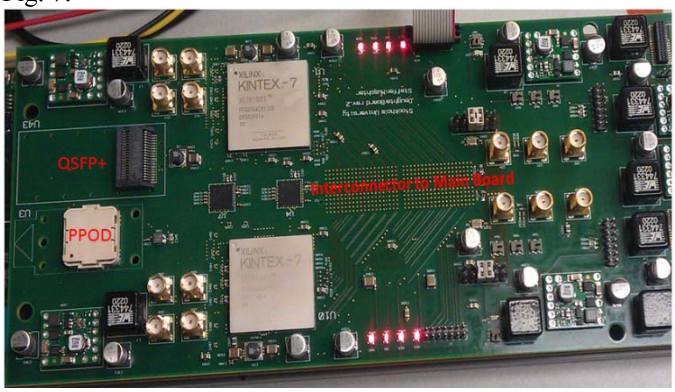

Fig. 7. The second prototype of the Daughter Board.

The QSFP+ module has passed the radiation test and has a sufficient capability to handle the required data rates; thus the third generation of the Daughter Board will no longer use PPOD links.

D. Super ReadOut Driver

The Super ReadOut Driver (sROD) for the Demonstrator project has been designed by Universidad de Valencia for data acquisition, data reconstruction and for providing digital information to the L1Calo trigger system [14].

The sROD module will implement commands to synchronize the new readout chain with the present data acquisition system. The sROD module will also communicate with the on-detector electronics to transmit control commands and reconfigure electronics settings, for example, to provide parameters to configure the analog Front-End Boards, Main Boards and Daughter Boards, and detector control commands to control the high voltage power supplies which feed the PMTs. Moreover, the sROD module will include preprocessor functionalities for pulse recognition, feature extraction, cell summation and merging, required to send trigger data to the L1Calo system.

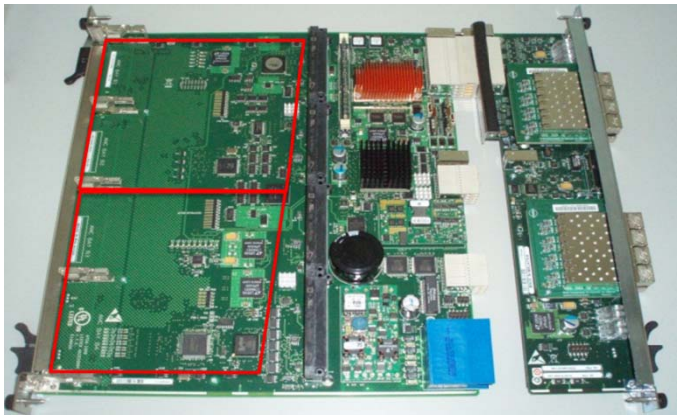

Fig. 8. A prototype of the sROD platform.

As shown in Fig. 8, the sROD is a double mid-size Advanced Mezzanine Card designed to be plugged into an Advanced Telecommunications Computing Architecture (ATCA) carrier or in a Micro Telecommunications Computing Architecture (μTCA) system. It includes one Xilinx Virtex 7 and one Kintex 7 FPGA as processing devices. Four QSFP+ modules are used to communicate with the Daughter Boards. The first prototype of the sROD module will be available by the end of summer 2013.

III. The TileCal Demonstrator System Tests

The Main Board and Daughter Board performance tests have started in fall 2013. A test setup for the Demonstrator prototyping electronics is shown in Fig. 9.

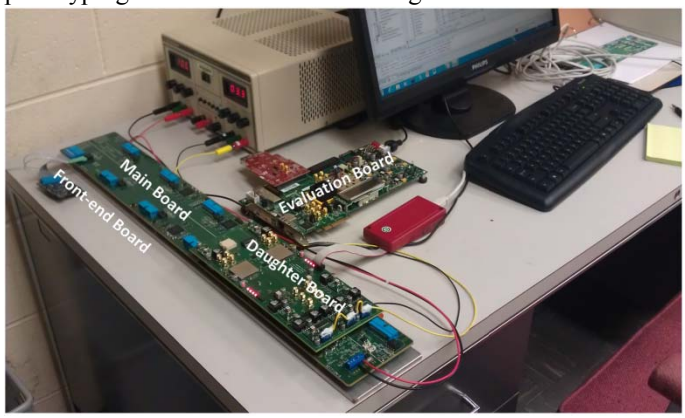

Fig. 9. A testing setup of the Demonstrator prototyping electronics.

The full function firmware test of the Main Board and the Daughter Board are expected to be accomplished in winter 2013. Demonstrator system tests with the entire on-detector and off-detector electronics, including 48 Analog Front-end Boards, 4 Main Boards, 4 Daughter Boards and two sRODs modules can be started early 2014.

IV. The TileCal Demonstrator Radiation Tests

A series of radiation tests are planned for mid of 2014 after the system performance and functionalities have been tested and the requirements are met. The required radiation tolerance for the TileCal on-detector electronics is ~40krad at HL-LHC [15]-[17]. The University of Chicago and Argonne National Laboratory have performed several radiation tests and studies for the Analog Front-End Board, as well as the active components on the Main Board and the Daughter Board. Some of the weak components found in DC regulators after the radiation tests have been replaced with qualified components.

V. Summary

Aiming to design a new readout and data acquisition system for Phase II TileCal upgrade, a Demonstrator with a completely re-designed electronics, using new commercially available off-the-shelf advanced components has been built. The system has a 17-bit dynamic range with a good signal to noise ratio to readout PMT signals. It is capable of delivering both analog (for compatibility with present system) and fully digital L1Calo trigger signals. The goal for the Demonstrator project is to understand the design challenges in the future Phase II upgrade, and gain some field experience, especially with the low noise readout front-end electronics design, digital trigger implementations and to evaluate different trigger algorithms. This work will greatly benefit the future upgrade design tasks for TileCal.

VI. Acknowledgement

This work is a collective effort of the TileCal upgrade collaboration; we wish to take this opportunity to extend our sincere thanks to Augusto Cerqueira, Ferran Granena, Juan Ferrer, James Proudfoot, Carlos Solans, Julio Souza and many other participants in the TileCal Demonstrator project.

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