Proposal of Delay Line Readout with 40-GHz Analog Sampler for Large Scale Pico-second TOF Detectors

PSEC Collaboration

March 4 2008
System Diagram of Delay Line Readout with Analog Sampler

Total Electronics Channels per MCP-PMT:
32 delay line readout channels
1 reference channel
Principle of Delay Line Readout

Timing:
(Overtop sampling)

Position:

Energy:
(Full Waveform Sampling)

\[ t_0 = \frac{t_1 + t_2}{2} \]

\[ x_i = \frac{t_1 - t_2}{t_1 + t_2} \]

\[ E_i = q_1 + q_2 \]

In next plan, no stub pads along the lines MCP
Proposed Anode Board with Existed 1024-anode Tube (bottom review)

Temporary test:
With elastomer contacting to the anode pads

16 x 2” Z=50Ω Lines
Proposed Anode Board with Existed 1024-anode Tube (top review)

Ground Plane

64 ball-contacts feed signal to front-end electronics board
Front-end Electronics Board (top review)

64 ball-contacting pads on bottom side receive signals from anode board

33-CH 40Ghz Analog Sampler Chip

FPGA

Cable Conn
Estimating the effects of distributed stub capacitive loads

Short stub \((\Delta t < 0.5 t_{\text{rise}})\) connected uniformly distributed can be modeled as T line with effective line parameters

\[
Z_0' = \sqrt{\frac{L}{C + \alpha C_L}} \quad V_p' = \sqrt{\frac{1}{L(C + \alpha C_L)}}
\]

\(L, C\) are unit-length parameters of the line, \(\alpha\) is capacitance distribution coefficient

\[
\alpha = \frac{\text{Number}}{\text{Length}}
\]

F.Tang
Equal distributed $33 \ C_L = 200f$ along 2-inch line, it causes impedance reduced to $Z'$, however, it also reduced the BW.

$$Z' = \sqrt{\frac{L}{C + \alpha C_L}}$$

$$\alpha = \frac{nC_L}{\text{Length}}$$

$$\alpha C_L = 3.3 \ p$$

$$Tr = 2.2\tau = 2.2 \frac{Z_0}{2} \alpha C_L = 181.5\ ps$$

$$BW \approx 1.93\ GHz$$

F. Tang
Single Channel Delay Line Readout Modeling

Stimulus: \( tr = tf = 200 \text{ps} \) at pads #5

DL_left (t1)

DL_right (t2)
Waveforms on Both Ends

Waveform on DL_left (t1)

Waveform on DL_right (t2)
Interconnection between MCP-PMT and Electronics Board

- MCP-PMT
- Microstrip Delay Line Anodes
- Cherenkov light
- Ball-contacts
- Vias
- Ground
- HV1
- HV2
- HV3
- GND
- LV
- Front-end Electronics Board
- Sampler Chip
Modeling of Interconnection between Microstrip Delay Line Anodes and Sampler

Impedance discontinuity caused by vias and ball contacts

C=150f for a via of 15x10x5
L=0.3n for a via of h=62, d=10
Zvia=31.6ohm
Summary

- Timing, position and energy information (more applications)
- Less readout electronics channels
- More signal collector areas (higher efficient)
- Matched impedance all the way to the chip
- Higher signal bandwidth
- Easier anode board layout
- Easier interconnection between the anode and the electronics board

- Prototype with 2 LAB2 or 2 DRS4 Chip
  (May be 2X interleaving)

- Built-in microstrip delay line anodes to get rid of anode stubs. (no external anode board needed!)