



# 2M x 8 Static RAM

## Features

- High speed
  - $t_{AA} = 8, 10, 12 \text{ ns}$
- Low active power
  - 1080 mW (max.)
- Operating voltages of  $3.3 \pm 0.3V$
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$  and  $\overline{CE}_2$  features

## Functional Description

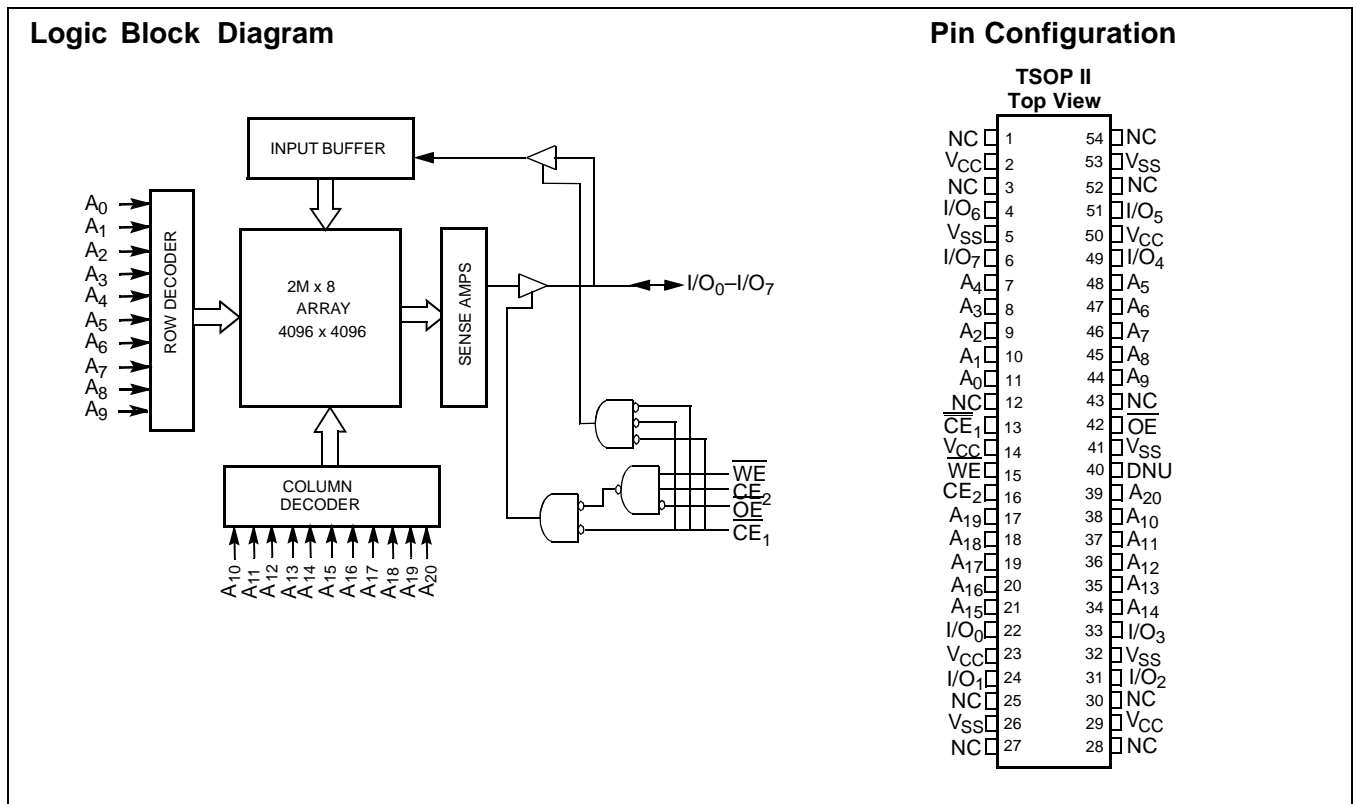
The CY7C1069AV33 is a high-performance CMOS Static RAM organized as 2,097,152 words by 8 bits. Writing to the

device is accomplished by enabling the chip (by taking  $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) and Write Enable ( $\overline{WE}$ ) inputs LOW.

Reading from the device is accomplished by enabling the chip ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) as well as forcing the Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a Write operation ( $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH, and  $\overline{WE}$  LOW).

The CY7C1069AV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and a 48-ball fine-pitch ball grid array (FBGA) package.

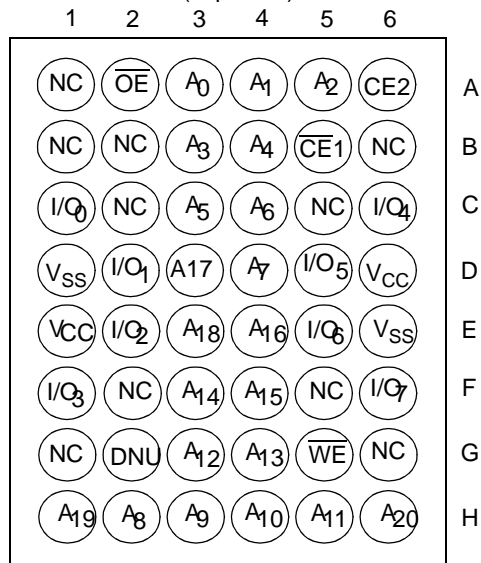


## Selection Guide

		-8	-10	-12	Unit
Maximum Access Time		8	10	12	ns
Maximum Operating Current	Commercial	300	275	260	mA
	Industrial	300	275	260	
Maximum CMOS Standby Current	Commercial/Industrial	50	50	50	mA

**Pin Configurations**
**48-ball FBGA**

(Top View)





**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....-65°C to +150°C

Ambient Temperature with Power Applied.....-55°C to +125°C

Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> .... -0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State<sup>[1]</sup> .....-0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

Current into Outputs (LOW)..... 20 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

**DC Electrical Characteristics** Over the Operating Range

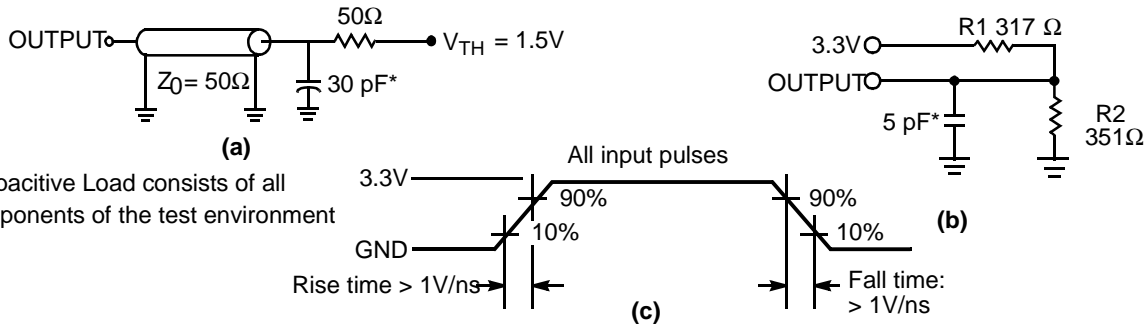
Parameter	Description	Test Conditions	-8		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	-1	+1	µA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	-1	+1	-1	+1	µA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Commercial	300		275		260	mA
			Industrial	300		275		260	mA
I <sub>SB1</sub>	Automatic CE Power-down Current —TTL Inputs	CE <sub>2</sub> ≤ V <sub>IL</sub> , Max. V <sub>CC</sub> , SCE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		70		70		70	mA
I <sub>SB2</sub>	Automatic CE Power-down Current —CMOS Inputs	CE <sub>2</sub> ≤ 0.3V, Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		50		50		50	mA

**Capacitance<sup>[2]</sup>**

Parameter	Package	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Z54	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	6	pF
	BA48			8	pF
C <sub>OUT</sub>	Z54	I/O Capacitance		8	pF
	BA48			10	pF

**Notes:**

- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms<sup>[3]</sup>**


\*Capacitive Load consists of all components of the test environment

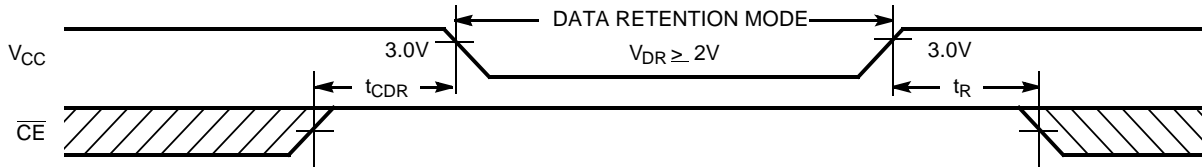
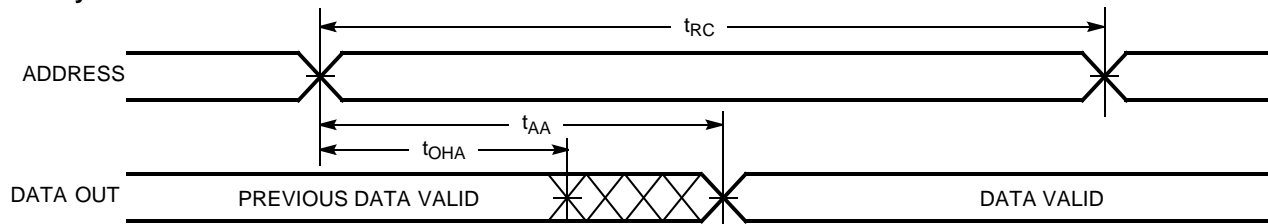
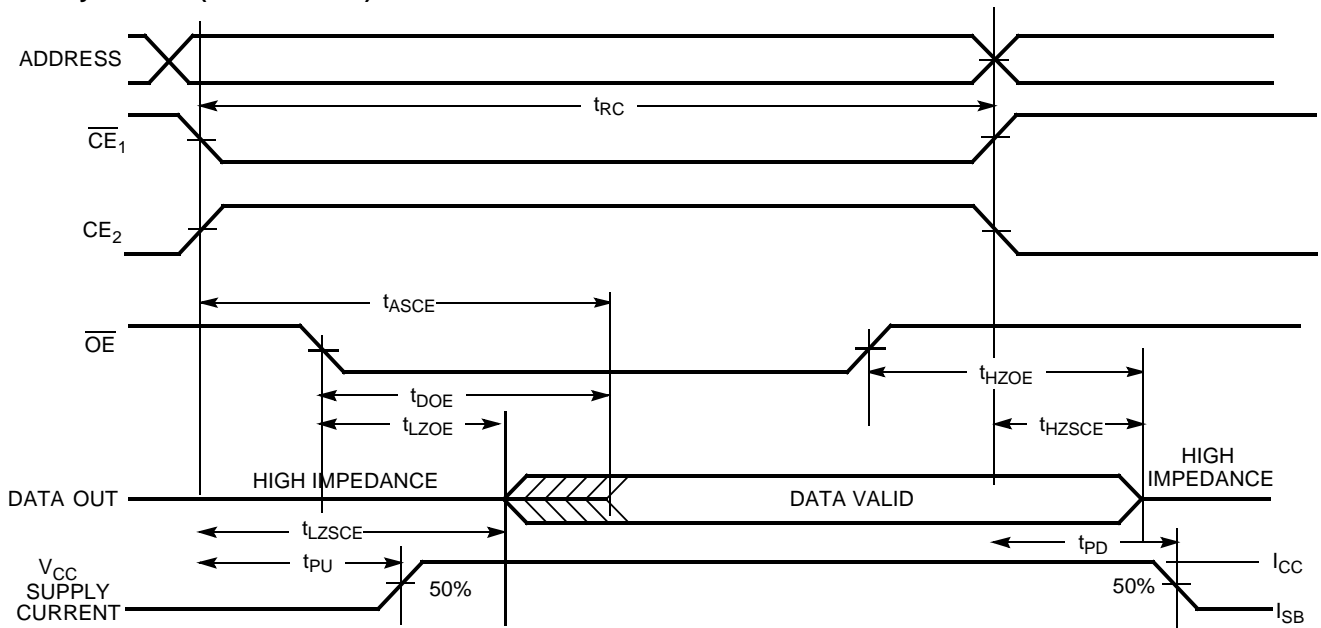
\*Including jig and scope

**AC Switching Characteristics Over the Operating Range<sup>[4]</sup>**

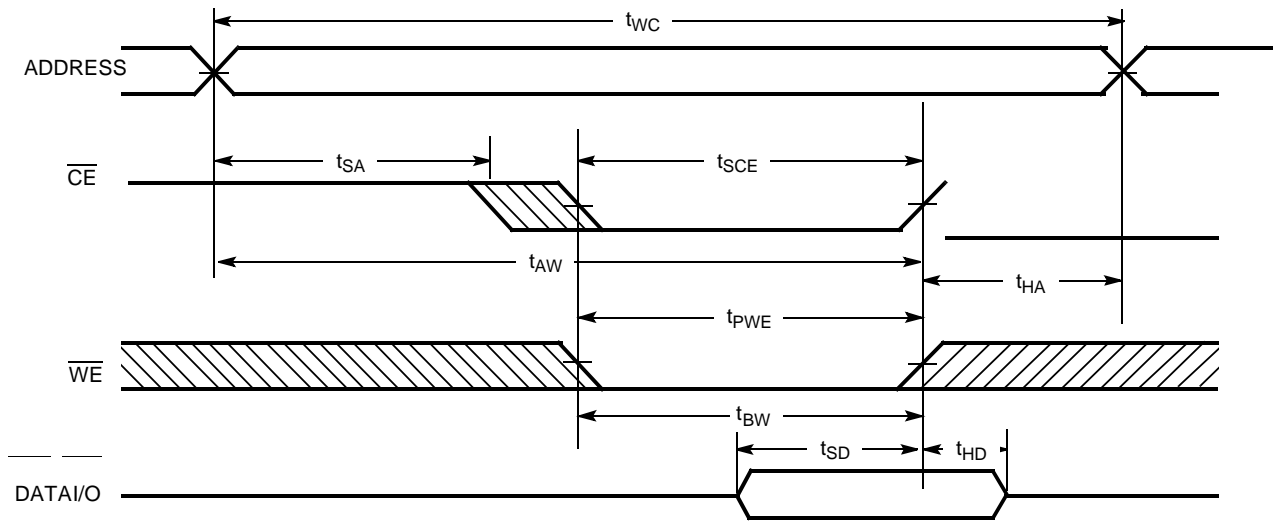
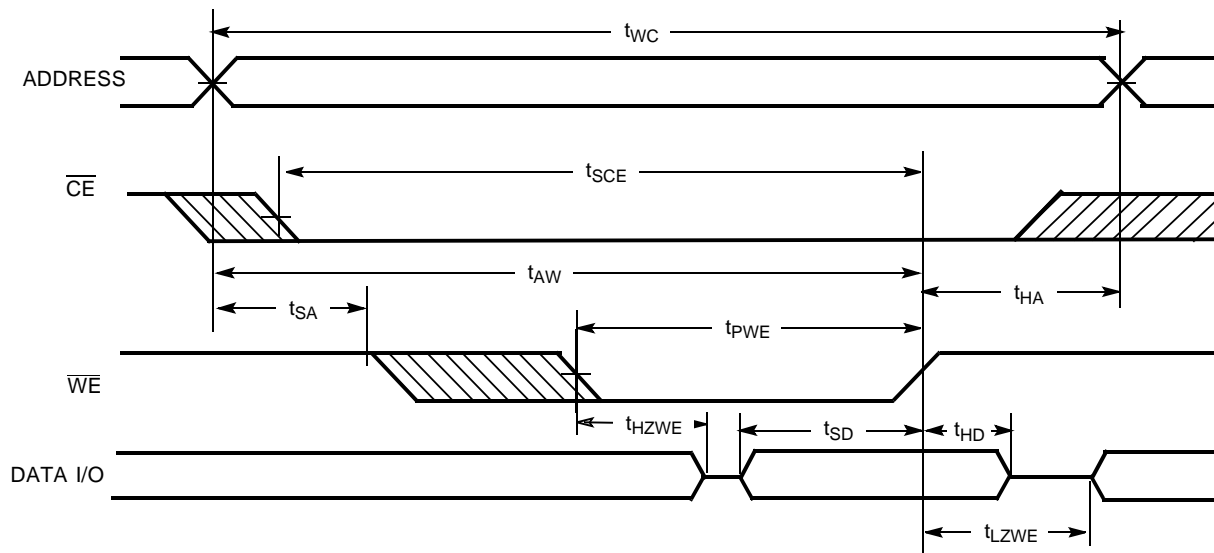
Parameter	Description	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
$t_{\text{power}}$	$V_{CC}(\text{typical})$ to the First Access <sup>[5]</sup>	1		1		1		ms
$t_{\text{RC}}$	Read Cycle Time	8		10		12		ns
$t_{\text{AA}}$	Address to Data Valid		10		10		12	ns
$t_{\text{OHA}}$	Data Hold from Address Change	3		3		3		ns
$t_{\text{ACE}}$	$\overline{\text{CE}}_1$ LOW/ $\text{CE}_2$ HIGH to Data Valid		8		10		12	ns
$t_{\text{DOE}}$	$\text{OE}$ LOW to Data Valid		5		5		6	ns
$t_{\text{LZOE}}$	$\text{OE}$ LOW to Low-Z <sup>[6]</sup>	1		1		1		ns
$t_{\text{HZOE}}$	$\text{OE}$ HIGH to High-Z <sup>[6]</sup>		5		5		6	ns
$t_{\text{LZCE}}$	$\overline{\text{CE}}_1$ LOW/ $\text{CE}_2$ HIGH to Low-Z <sup>[6]</sup>	3		3		3		ns
$t_{\text{HZCE}}$	$\overline{\text{CE}}_1$ HIGH/ $\text{CE}_2$ LOW to High-Z <sup>[6]</sup>		5		5		6	ns
$t_{\text{PU}}$	$\overline{\text{CE}}_1$ LOW/ $\text{CE}_2$ HIGH to Power-up <sup>[7]</sup>	0		0		0		ns
$t_{\text{PD}}$	$\overline{\text{CE}}_1$ HIGH/ $\text{CE}_2$ LOW to Power-down <sup>[7]</sup>		8		10		12	ns
<b>Write Cycle<sup>[8, 9]</sup></b>								
$t_{\text{WC}}$	Write Cycle Time	8		10		12		ns
$t_{\text{SCE}}$	$\overline{\text{CE}}_1$ LOW/ $\text{CE}_2$ HIGH to Write End	6		7		8		ns
$t_{\text{AW}}$	Address Set-up to Write End	6		7		8		ns
$t_{\text{HA}}$	Address Hold from Write End	0		0		0		ns
$t_{\text{SA}}$	Address Set-up to Write Start	0		0		0		ns
$t_{\text{PWE}}$	WE Pulse Width	6		7		8		ns
$t_{\text{SD}}$	Data Set-up to Write End	5		5.5		6		ns
$t_{\text{HD}}$	Data Hold from Write End	0		0		0		ns
$t_{\text{LZWE}}$	WE HIGH to Low-Z <sup>[6]</sup>	3		3		3		ns
$t_{\text{HZWE}}$	WE LOW to High-Z <sup>[6]</sup>		5		5		6	ns

**Notes:**

- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0V). As soon as 1ms ( $T_{\text{power}}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation can begin including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0V) voltage.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
- This part has a voltage regulator which steps down the voltage from 3V to 2V internally.  $t_{\text{power}}$  time has to be provided initially before a Read/Write operation is started.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZSCE}}$ ,  $t_{\text{HZWE}}$  and  $t_{\text{LZOE}}$ ,  $t_{\text{LZCE}}$ , and  $t_{\text{LZWE}}$  are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{\text{CE}}_1$  LOW /  $\text{CE}_2$  HIGH, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}_1$  and  $\overline{\text{WE}}$  must be LOW along with  $\text{CE}_2$  HIGH to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\text{OE}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No. 1<sup>[10, 11]</sup>**

**Read Cycle No. 2 ( $\overline{OE}$  Controlled) [11, 12]**

**Notes:**

10. Device is continuously selected.  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
11.  $\overline{WE}$  is HIGH for Read cycle.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{CE}_1$  Controlled)**<sup>[13, 14, 15]</sup>

**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)**<sup>[13, 14, 15]</sup>

**Truth Table**

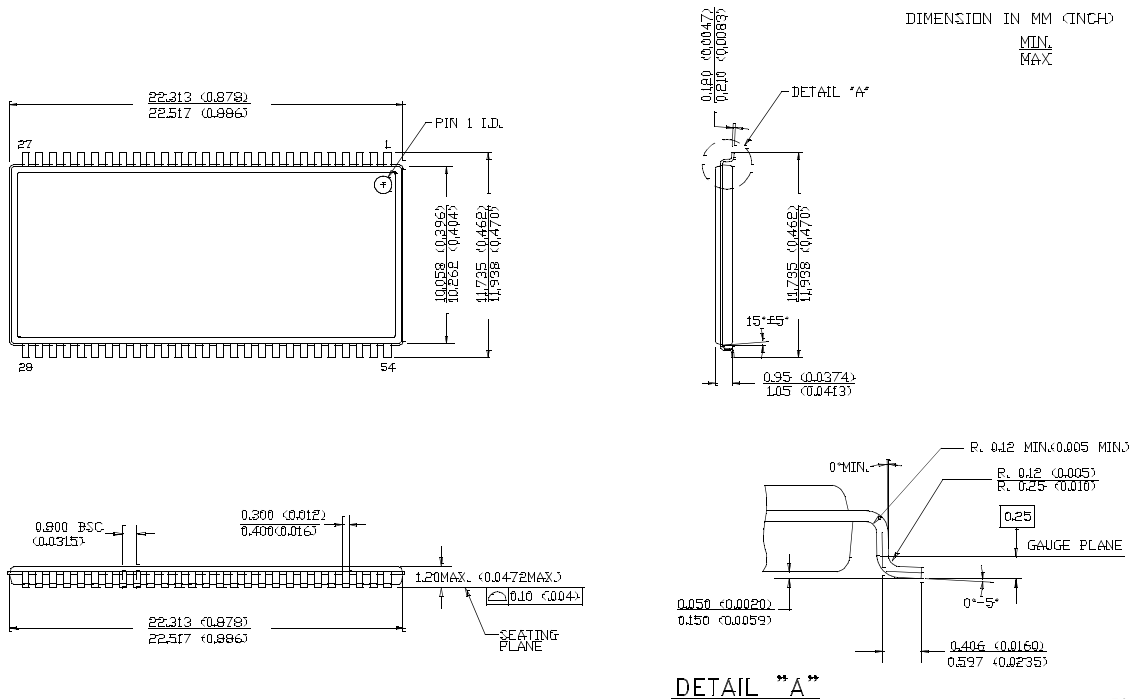
$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	Mode	Power
H	X	X	X	High-Z	Power-down	Standby ( $I_{SB}$ )
X	L	X	X	High-Z	Power-down	Standby ( $I_{SB}$ )
L	H	L	H	Data Out	Read All Bits	Active ( $I_{CC}$ )
L	H	X	L	Data In	Write All Bits	Active ( $I_{CC}$ )
L	H	H	H	High-Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Notes:**

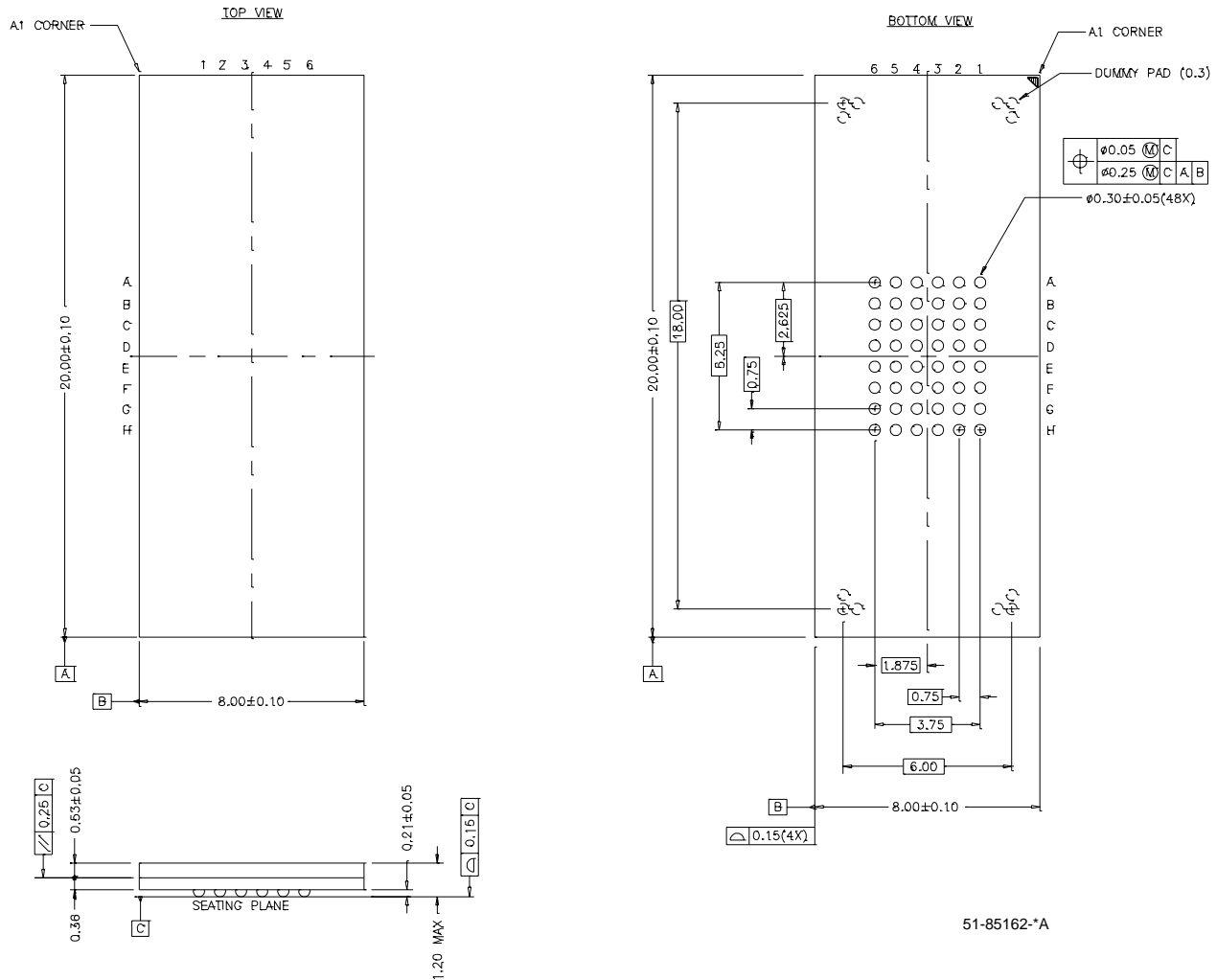
12. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $\overline{CE}_2$  transition HIGH.
13. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}_1$  goes HIGH /  $\overline{CE}_2$  LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
15.  $\overline{CE}$  above is defined as a combination of  $\overline{CE}_1$  and  $\overline{CE}_2$ . It is active low.

**Ordering Information**

Speed (ns)	Ordering Code <sup>[16]</sup>	Package Name	Package Type	Operating Range
8	CY7C1069AV33-8ZC	Z54	54-pin TSOP II	Commercial
	CY7C1069AV33-8ZI			Industrial
	CY7C1069AV33-8BAC	BA48	48-ball Mini BGA	Commercial
	CY7C1069AV33-8BAI			Industrial
10	CY7C1069AV33-10ZC	Z54	54-pin TSOP II	Commercial
	CY7C1069AV33-10ZI			Industrial
	CY7C1069AV33-10BAC	BA48	48-ball Mini BGA	Commercial
	CY7C1069AV33-10BAI			Industrial
12	CY7C1069AV33-12ZC	Z54	54-pin TSOP II	Commercial
	CY7C1069AV33-12ZI			Industrial
	CY7C1069AV33-12BAC	BA48	48-ball Mini BGA	Commercial
	CY7C1069AV33-12BAI			Industrial

**Package Diagrams**
**54-lead Thin Small Outline Package, Type II Z54-II**

**Note:**

16. Contact a Cypress Representative for availability of the 48-ball Mini BGA (BA48) package.

**Package Diagrams (continued)**
**48-ball (8 mm x 20 mm x 1.2 mm) FBGA BA48G**


All product and company names mentioned in this document may be the trademarks of their respective holders.



**Document History Page**

Document Title: CY7C1069AV33 2M x 8 Static RAM				
Document Number: 38-05255				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	113724	03/27/02	NSL	New Data Sheet
*A	117060	07/31/02	DFP	Removed 15-ns bin
*B	117990	08/30/02	DFP	Added 8-ns bin Changing I <sub>CC</sub> for 8, 10, 12 bins t <sub>power</sub> changed from 1 μs to 1 ms Load Cap Comment changed (for Tx line load) t <sub>SD</sub> changed to 5.5 ns for the 10-ns bin Changed some 8-ns bin #'s (t <sub>HZ</sub> , t <sub>DOE</sub> , t <sub>DBE</sub> ) Removed hz < lz comments
*C	120385	11/13/02	DFP	Final Data Sheet Added note 4 to "AC Test Loads and Waveforms" and note 7 to t <sub>pu</sub> and t <sub>pd</sub> Updated Input/Output Caps (for 48BGA only) to 8 pf/10 pf and for the 54-pin TSOP to 6/8 pf
*D	124441	2/25/03	MEG	Changed ISB1 from 100 mA to 70 mA Shaded the 48fBGA product offering information