# SVT UPGRADE: Memory Cards Designs

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# *SVT UPGRADE: INTRODUCTION*

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## SVT upgrade implemented in Pulsar Board

❖ *3 types of* **Firmware** *and their* **Memory** *requirements*

✓ ***AMS/RW***

**SSmap:** ***128k x 12bits*** **(17-bit addr x 12-bit data)**

**AMmap:** ***1M x 36bits*** **(20-bit addr x 36-bit data)**

✓ ***HB***

**SSmap:** ***128k x 12bits*** **(17-bit addr x 12-bit data)**

**AMmap:** ***1M x 36bits*** **(20-bit addr x 36-bit data)**

**HLM:** ***256k x 21bits*** **(18-bit addr x 21-bit data)**

**HCM:** ***32k x 4bits*** **(15-bit addr x 4-bit data)**

✓ ***TF***

**Intercept:** ***4M x 42bits*** **(22-bit addr x 42-bit data)**

**SSmap:** ***512k x 24bits*** **(19-bit addr x 24-bit data)**

# *SVT UPGRADE: System Configurations*

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- **2 types of mezzanine memory cards fit all**

**(1) M4M: 4M x 48bits memory card**

**(2) M512K: 512K x 24bits memory card**

## System Configurations:

| Mezzanine | HB | AMS/RW | TF |
|---|---|---|---|
| M4M | AMmap/SSmap | AMmap | Intercept1 |
| M512 | HLM | SSmap | SSmap |
| M4M | None | None | Intercept2 |
| M512 | None | None | SSmap |

# M4M MEMORY CARD DIAGRAM

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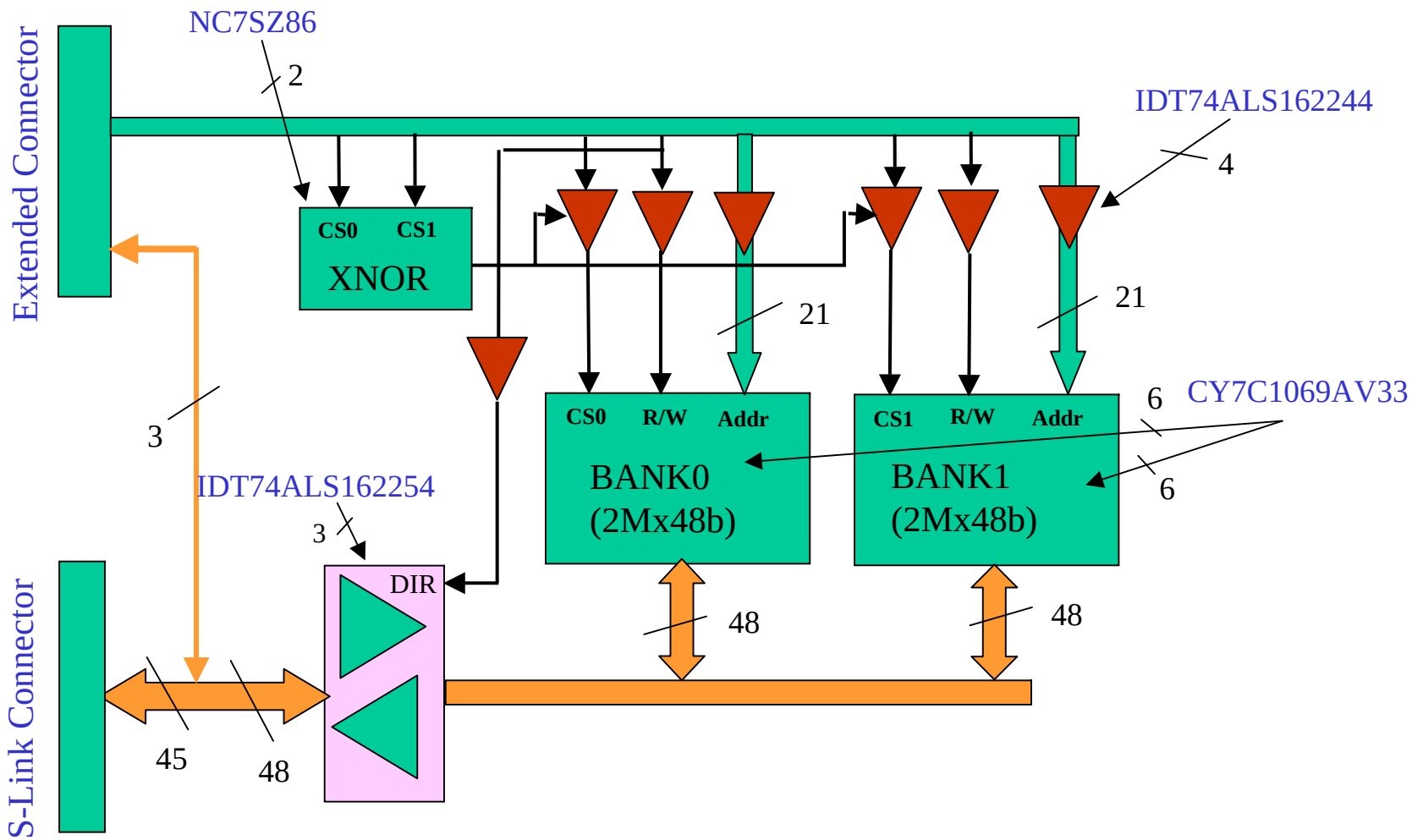


4Mx48bits Mezzanine Memory Card Diagram

# Memory Access Speed

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## M4M Memory Access Speed

**Single word write-then-read or read-then-write: ~40Mhz**

**T = T(flight_max) + Tpd (addr_buffer) + Tpd(data_buffer)**

**+ T(fpga_setup) + T(mem_access) + T(skew_margin)**

**= 3.6ns + 3ns + 3ns + 4ns + 10ns + 2ns = 24.6ns (~40Mhz)**

**Multiple write or multiple read: ~60Mhz**

**T= T(mem_access) + T(fpga_setup) + T(skew_margin)**

**= 10ns + 4ns + 2ns = 16ns (~60Mhz)**

**Latency: ~25ns**

# MEMORY WRITE TIMING

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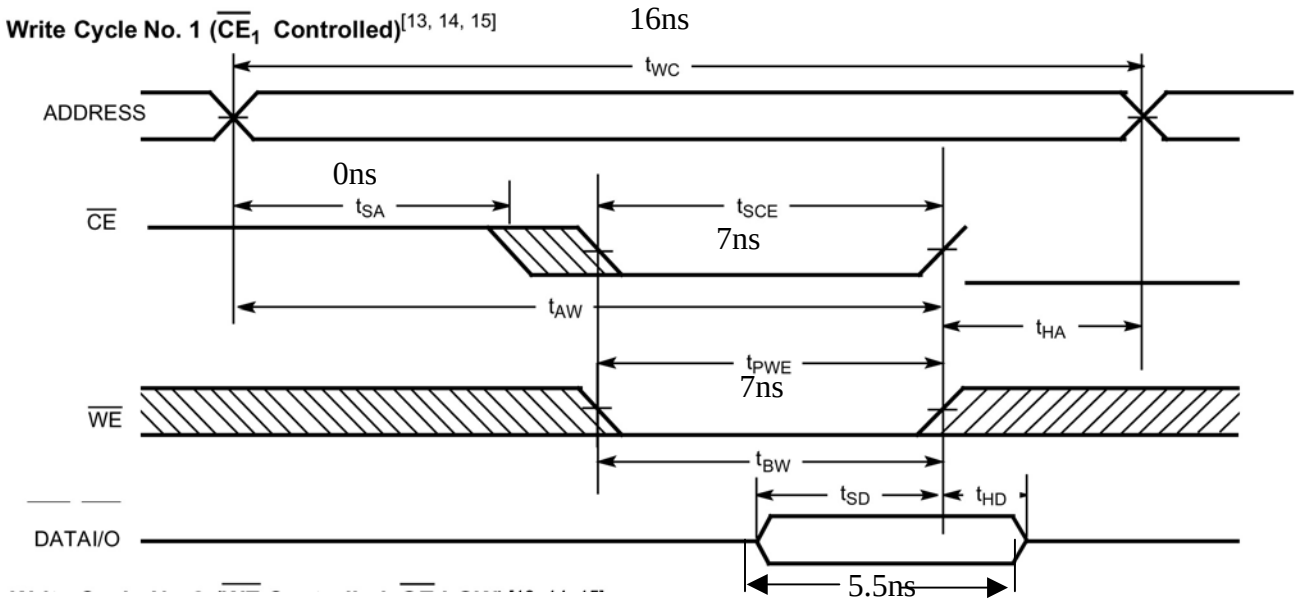
## Multiple Write Timing



# MEMORY READ TIMING

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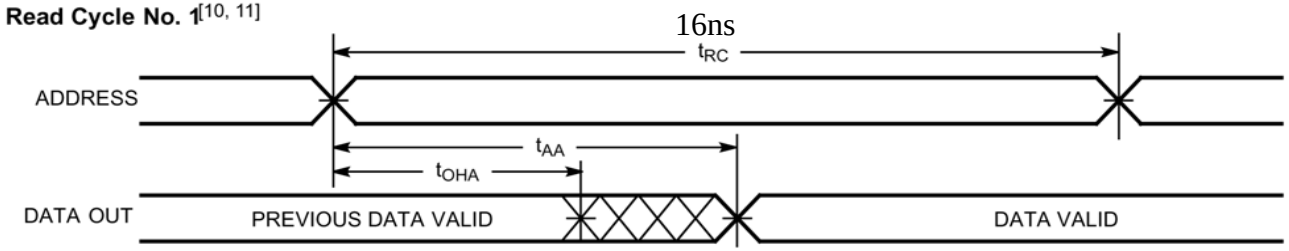
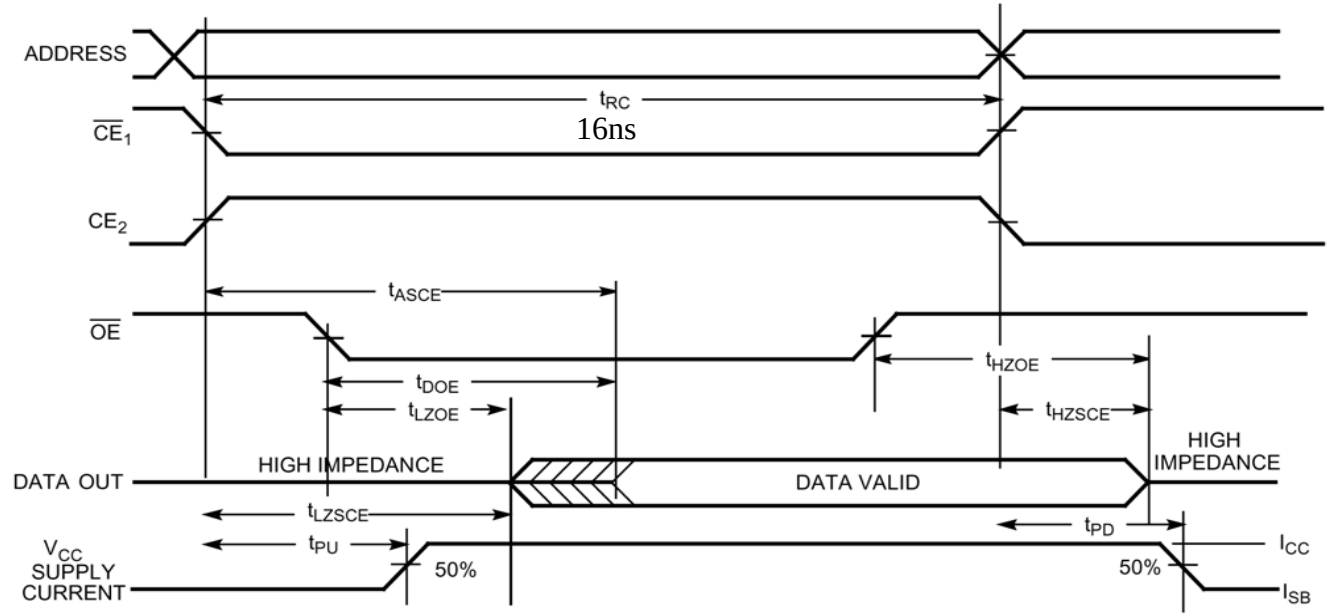
## *Multiple Read Timing*

**Read Cycle No. 1** [10, 11]




**Read Cycle No. 2 ($\overline{OE}$ Controlled)** [11, 12]




**Notes:**

10. Device is continuously selected. $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
11. $\overline{WE}$ is HIGH for Read cycle.

# *POWER CONSUMPTION*

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**Single Power Supply: +3.3V**

**Standby: 1.3A**

**Full Speed Operation: 3A**

# Board Layout Techniques

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## ➢ Difficulty and Challenge:

*Maximum Length of Address and Data Lines: 9 inch*

*Way long compare with "Critical Length"  L= Tr/2Tpd*

***All Address and data line need to be well terminated.***

## ➢ Termination Methods:

*Address Lines  (IDT74ALVC162244) :*

**Inputs:**  ***Built-in diode clamping*** (from Pulsar)

**Outputs:** ***Built-in source series terminators*** (to SRAMs)

*Data Lines (IDT74ALVC162245) :*

**All Inputs:**  ***Built-in diode clamping***

**B-port Outputs:** ***External source series terminators*** (to Pulsar)

**A-port Outputs:** ***Built-in source series terminators*** (to SRAMs)

# Board Layout Techniques

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- ***Board Layers: 8***
  **4 signal layers**
  **4 power layers**

- ***To acchieve optimal system performance***
  - ✓ **Double side placement: Bank0 on top, Bank1 on Bottom.**
  - ✓ **Swap Bank0 and Bank1 Address and Data pin orders to share vias that greatly reduce route length and avoid T-junctions**
  - ✓ **Short trace to reduce time of flight**
  - ✓ **Terminate lines to increase signal integrity**
  - ✓ **Group Address and Data lines for better routing**
  - ✓ **Place different group wires in different layers to reduce cross talk**
  - ✓ **Place decoupling capacitors to reduce power supply and circuit switch noise**
  - ✓ **Obey EMC/EMI rules to avoid signal cross talk and reduce system noise**
  - ✓ **All trace are impedance controlled (50 ohms)**

# Board Stack Order and Layer Thickness

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| B2555 Board Stack Order and Layer Thickness Table | | | | |
|---|---|---|---|---|
| Layer# | Material Type | Description | Thickness (mil) | Impedance |
| Layer1 (Artwork_1) | Conductive(top, Signal_1) | Microstrip | 1.4 | 52 |
| | Dielectric 4.7 | | 4 | |
| Layer2 (Artwork_2) | Conductive(VCC) | Plane | 2.8 | |
| | Dielectric 4.7 | | 9 | |
| Layer3 (Artwork_3) | Conductive (Signal_3) | Stripline | 1.4 | 53 |
| | Dielectric 4.7 | | 9 | |
| Layer4 (Artwork_4) | Conductive (GROUND) | Plane | 2.8 | |
| | Dielectric 4.7 | | 4 | |
| Layer5 (Artwork_5) | Conductive (VCC) | Plane | 2.8 | |
| | Dielectric 4.7 | | 9 | |
| Layer6 (Artwork_6) | Conductive (signal_4) | Stripline | 1.4 | 53 |
| | Dielectric 4.7 | | 9 | |
| Layer7 (Artwork_7) | Conductive (Ground) | Plane | 2.8 | |
| | Dielectric 4.7 | | 4 | |
| Layer8 (Artwork_8) | Conductiive (Bottom, Signal_2) | Microstrip | 1.4 | 52 |

Note: [1] Total Board Thickness is 0.062 inch, +/- 0.010 inch
[2] Above is recommended layer thickness based on FR4 with dielectric constant 4.7.
[3] Vendor has a right to adjust layer thickness and control all layer impedance at 50 ohms with tolerance less than +/- 10%.

**Add extra power layer pair (layer4, Layer5)**

**(1) Acts as a distributed decoupling capacitor on entire board**

**(2) Isolates signal layers (layer3 and layer6) to reduce EMC/EMI emissions**

**(3) Increases ability to sink heat out of SRAM chips**

**(4) Decreases DC resistance and AC inductance**

# M4M Mezzanine Card Dimensions

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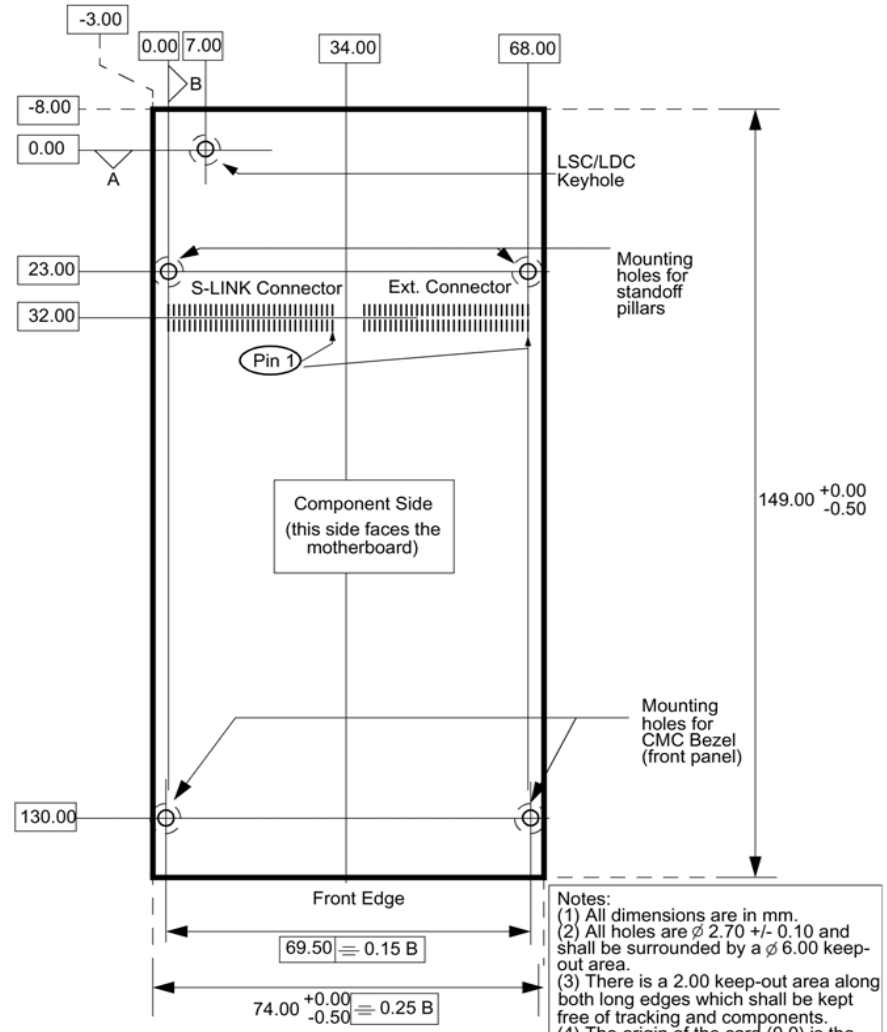

# M4M ON-BOARD LED DISPLAYS

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## M4M On-Board LED Displays

| FUNCTION | LED1 | LED2 | LED3 | LED4 | LED5 |
|---|---|---|---|---|---|
| POWER ON | ON | | | | |
| POWER OFF | OFF | | | | |
| | | | | | |
| BANK0_WRITE | | ON | OFF | ON | OFF |
| BANK0_READ | | OFF | ON | ON | OFF |
| BANK0_STANDBY | | X | X | OFF | X |
| | | | | | |
| BANK1_WRITE | | ON | OFF | OFF | ON |
| BANK1_READ | | OFF | ON | OFF | ON |
| BANK1_STANDBY | | X | X | X | OFF |

# Address or Data Waveforms @ Address or Data Buffer Inputs

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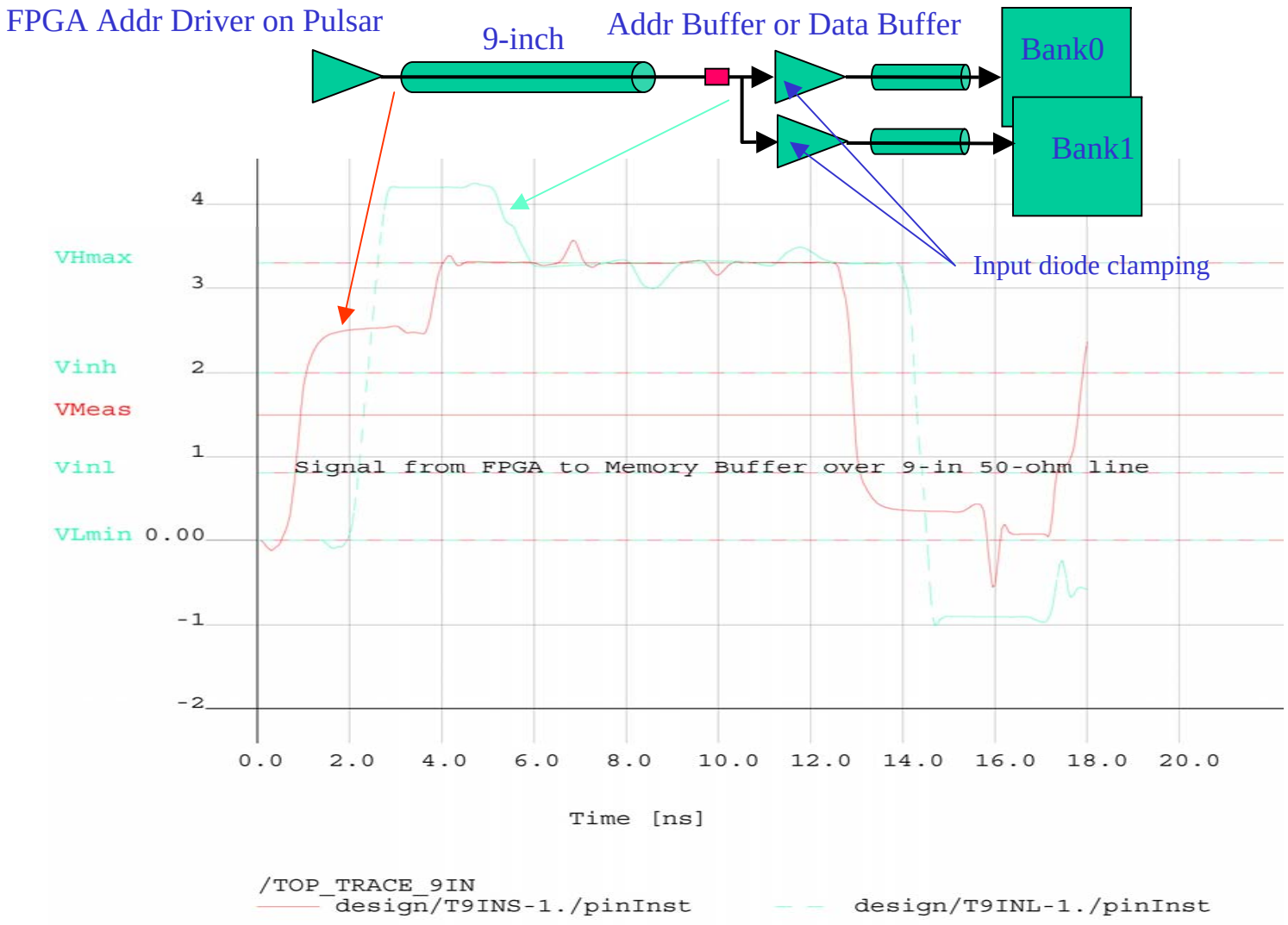

# Address Signal Waveforms at SRAM Inputs

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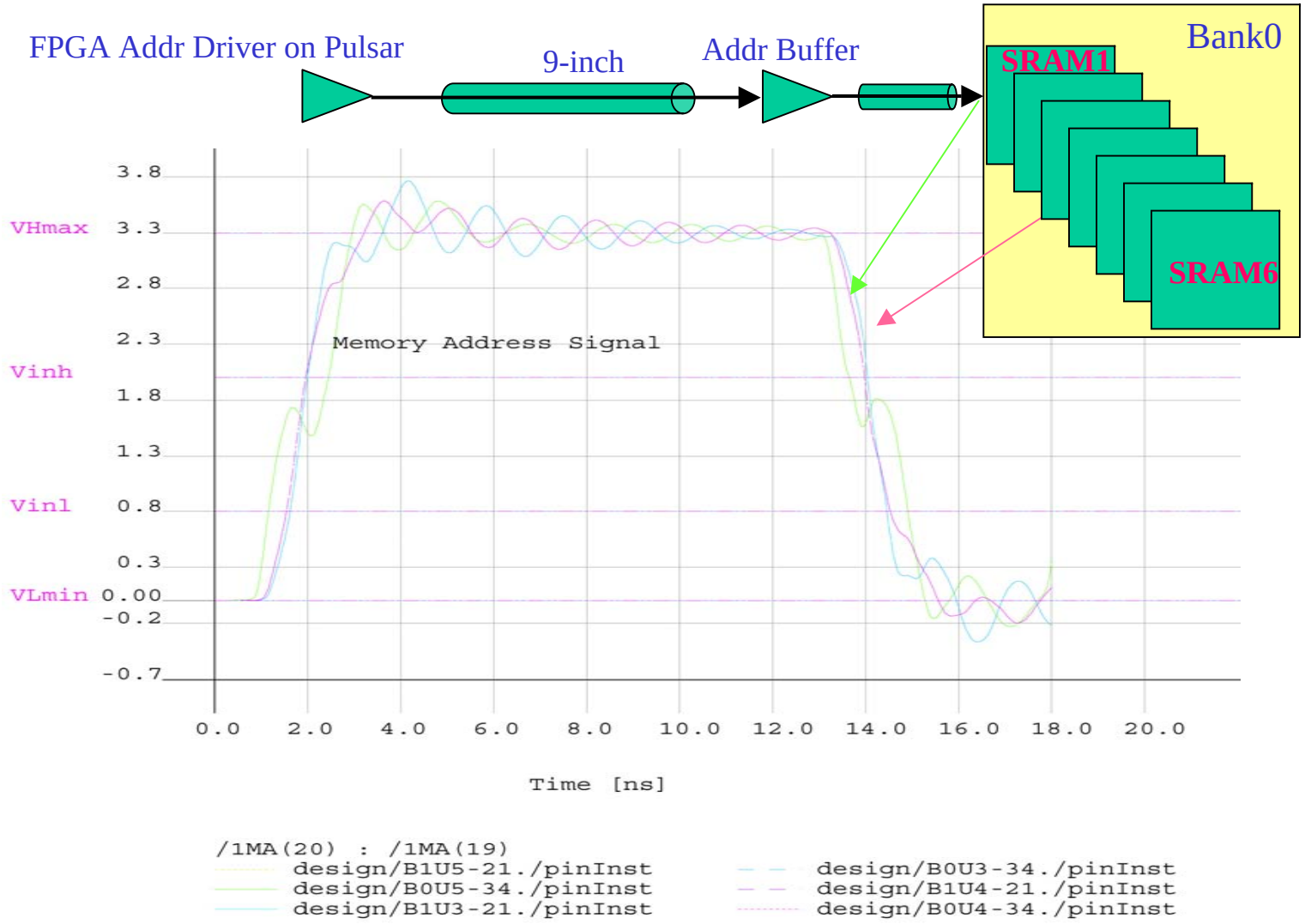

# Write Data Waveforms @ SRAM Inputs

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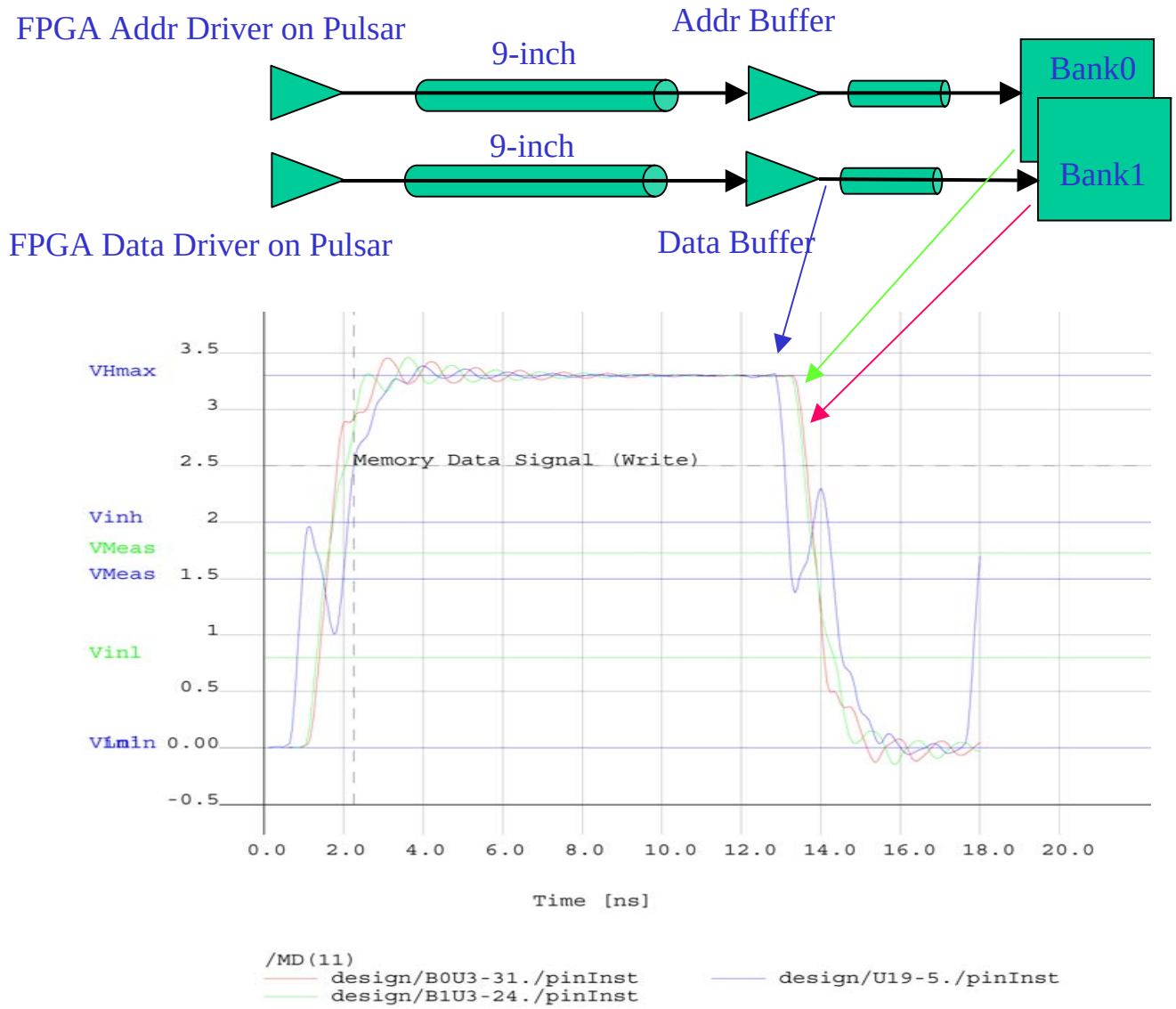

# Read Data Waveforms @Data Buffer Inputs

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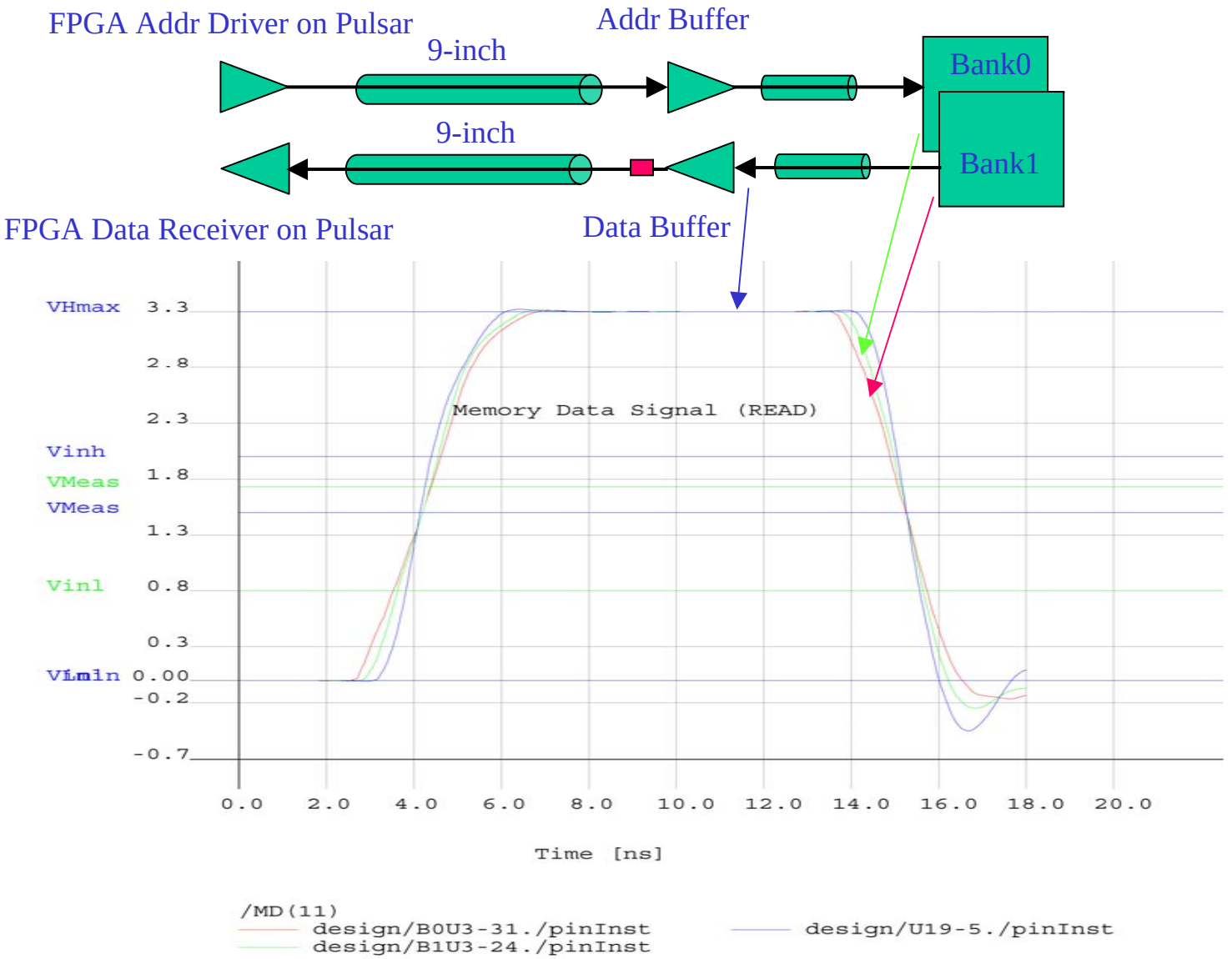

# Read Data Waveforms @ FPGA Inputs

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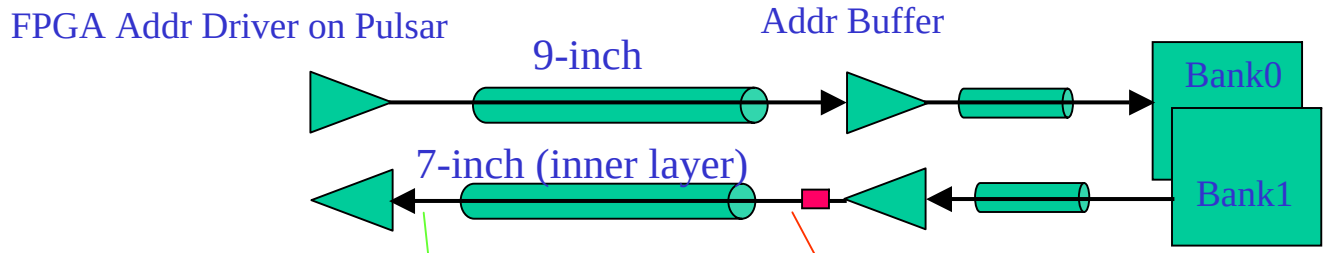


# *M4M Mezzanine Card Design Info Website*

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http://edg.uchicago.edu/~tang/Memory/sram_M4M.html