Design Team Members

Mel Shochet <shochet@hep.uchicago.edu>
Harold Sanders <harold@frodo.uchicago.edu>
Fukun Tang <tang@frodo.uchicago.edu>
Un-Ki Yang <ukyang@cdf.uchicago.edu>
Ivan Furic <ikfuric@hep.uchicago.edu>
Jahred Adelman <jahred@cdf.uchicago.edu>
Ted Liu <thliu@fnal.gov>
Takasumi Maruyama <maruyama@fnal.gov>
Paola Giannetti <paola.giannetti@pi.infn.it>
Alberto Annovi <alberto.annovi@pi.infn.it>
Franco Spinella <franco.spinella@pi.infn.it>
SVT upgrade implemented in Pulsar Board

- **3 types of Firmware and their Memory requirements**

  ✓ **AMS/RW**
  - SSmap: 128k x 12bits (17-bit addr x 12-bit data)
  - AMmap: 1M x 36bits (20-bit addr x 36-bit data)

  ✓ **HB**
  - SSmap: 128k x 12bits (17-bit addr x 12-bit data)
  - AMmap: 1M x 36bits (20-bit addr x 36-bit data)
  - HLM: 256k x 21bits (18-bit addr x 21-bit data)
  - HCM: 32k x 4bits (15-bit addr x 4-bit data)

  ✓ **TF**
  - Intercept: 4M x 42bits (22-bit addr x 42-bit data)
  - SSmap: 512k x 24bits (19-bit addr x 24-bit data)
2 types of mezzanine memory cards fit all

(1) M4M: 4M x 48bits memory card
(2) M512K: 512K x 24bits memory card

<table>
<thead>
<tr>
<th>Mezzanine</th>
<th>HB</th>
<th>AMS/RW</th>
<th>TF</th>
</tr>
</thead>
<tbody>
<tr>
<td>M4M</td>
<td>AMmap/SSmap</td>
<td>AMmap</td>
<td>Intercept1</td>
</tr>
<tr>
<td>M512</td>
<td>HLM</td>
<td>SSmap</td>
<td>SSmap</td>
</tr>
<tr>
<td>M4M</td>
<td>None</td>
<td>None</td>
<td>Intercept2</td>
</tr>
<tr>
<td>M512</td>
<td>None</td>
<td>None</td>
<td>SSmap</td>
</tr>
</tbody>
</table>
Introduction to TileCal Readout System

M4M MEMORY CARD DIAGRAM

Extended Connector

NC7SZ86

CS0  CS1

XNOR

IDT74ALS162244

21

3

2

4

BANK0
(2Mx48b)

BANK1
(2Mx48b)

S-Link Connector

IDT74ALS162254

3

21

48

45

48

3

48

4

6

6

4Mx48bits  Mezzanine Memory Card Diagram
**M4M Memory Access Speed**

Single word write-then-read or read-then-write:  ~40Mhz

\[
T = T(\text{flight\_max}) + T_{pd}(\text{addr\_buffer}) + T_{pd}(\text{data\_buffer})
+ T(\text{fpga\_setup}) + T(\text{mem\_access}) + T(\text{skew\_margin})
= 3.6ns + 3ns + 3ns + 4ns + 10ns + 2ns = 24.6ns (\sim 40Mhz)
\]

Multiple write or multiple read:  ~60Mhz

\[
T = T(\text{mem\_access}) + T(\text{fpga\_setup}) + T(\text{skew\_margin})
= 10ns + 4ns + 2ns = 16ns (\sim 60Mhz)
\]

Latency:  ~25ns
Multiple Write Timing

Write Cycle No. 1 (CE₁ Controlled)\textsuperscript{[13, 14, 15]}
**Multiple Read Timing**

**Read Cycle No. 1**\(^{10, 11}\)

- ADDRESS
- DATA OUT
- PREVIOUS DATA VALID
- DATA VALID

**Read Cycle No. 2 (OE Controlled)**\(^{11, 12}\)

- ADDRESS
- $\overline{OE}$
- $\overline{CE}_1$
- $CE_2$

**Notes:**

10. Device is continuously selected. $\overline{CE}_1 = V_h, \ CE_2 = V_h$.
11. WE is HIGH for Read cycle.
POWER CONSUMPTION

Single Power Supply: +3.3V

Standby: 1.3A

Full Speed Operation: 3A
Board Layout Techniques

Difficulty and Challenge:

Maximum Length of Address and Data Lines: 9 inch

Way long compare with “Critical Length” \( L = \frac{Tr}{2Tpd} \)

All Address and data line need to be well terminated.

Termination Methods:

Address Lines (IDT74ALVC162244):

Inputs: Built-in diode clamping (from Pulsar)

Outputs: Built-in source series terminators (to SRAMs)

Data Lines (IDT74ALVC162245):

All Inputs: Built-in diode clamping

B-port Outputs: External source series terminators (to Pulsar)

A-port Outputs: Built-in source series terminators (to SRAMs)
Board Layers:  8

- 4 signal layers
- 4 power layers

To achieve optimal system performance

- Double side placement: Bank0 on top, Bank1 on Bottom.
- Swap Bank0 and Bank1 Address and Data pin orders to share vias that greatly reduce route length and avoid T-junctions
- Short trace to reduce time of flight
- Terminate lines to increase signal integrity
- Group Address and Data lines for better routing
- Place different group wires in different layers to reduce cross talk
- Place decoupling capacitors to reduce power supply and circuit switch noise
- Obey EMC/EMI rules to avoid signal cross talk and reduce system noise
- All trace are impedance controlled (50 ohms)
Board Stack Order and Layer Thickness

<table>
<thead>
<tr>
<th>Layer#</th>
<th>Material Type</th>
<th>Description</th>
<th>Thickness (mil)</th>
<th>Impedance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer1</td>
<td>Conductive(top, Signal_1)</td>
<td>Microstrip</td>
<td>1.4</td>
<td>52</td>
</tr>
<tr>
<td></td>
<td>Dielectric 4.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layer2</td>
<td>Conductive(VCC)</td>
<td>Plane</td>
<td>2.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dielectric 4.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layer3</td>
<td>Conductive(Signal_3)</td>
<td>Stripline</td>
<td>1.4</td>
<td>53</td>
</tr>
<tr>
<td></td>
<td>Dielectric 4.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layer4</td>
<td>Conductive(GROUND)</td>
<td>Plane</td>
<td>2.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dielectric 4.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layer5</td>
<td>Conductive(VCC)</td>
<td>Plane</td>
<td>2.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dielectric 4.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layer6</td>
<td>Conductive(signal_4)</td>
<td>Stripline</td>
<td>1.4</td>
<td>53</td>
</tr>
<tr>
<td></td>
<td>Dielectric 4.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layer7</td>
<td>Conductive(Ground)</td>
<td>Plane</td>
<td>2.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dielectric 4.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Layer8</td>
<td>Conductive(Bottom, Signal_2)</td>
<td>Microstrip</td>
<td>1.4</td>
<td>52</td>
</tr>
</tbody>
</table>

Note: [1] Total Board Thickness is 0.062 inch, +/- 0.010 inch. 
[2] Above is recommended layer thickness based on FR4 with dielectric constant 4.7. 
[3] Vendor has a right to adjust layer thickness and control all layer impedance at 50 ohms with tolerance less than +/- 10%.

Add extra power layer pair (layer4, Layer5)

1) Acts as a distributed decoupling capacitor on entire board
2) Isolates signal layers (layer3 and layer6) to reduce EMC/EMI emissions
3) Increases ability to sink heat out of SRAM chips
4) Decreases DC resistance and AC inductance
Notes:
1. All dimensions are in mm.
2. All holes are Ø2.70 ± 0.10 and shall be surrounded by a Ø6.00 keep-out area.
3. There is a 2.00 keep-out area along both long edges which shall be kept free of tracking and components.
4. The origin of the card (0,0) is the centre of voltage keying hole.
## M4M On-Board LED Displays

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>LED1</th>
<th>LED2</th>
<th>LED3</th>
<th>LED4</th>
<th>LED5</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWER ON</td>
<td>ON</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>POWER OFF</td>
<td>OFF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BANK0_WRITE</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>BANK0_READ</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td></td>
</tr>
<tr>
<td>BANK0_STANDBY</td>
<td>X</td>
<td>X</td>
<td>OFF</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>BANK1_WRITE</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td>BANK1_READ</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td>BANK1_STANDBY</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>OFF</td>
</tr>
</tbody>
</table>
Address or Data Waveforms @ Address or Data Buffer Inputs

FPGA Addr Driver on Pulsar

9-inch Addr Buffer or Data Buffer

Bank0

Bank1

Input diode clamping

Signal from FPGA to memory buffer over 9-in 50-ohm line

Time [ns]

/TOP_TRACE_9IN
  design/T9INS-1../pinInst
  design/T9INL-1../pinInst
Address Signal Waveforms at SRAM Inputs

- FPGA Addr Driver on Pulsar
- 9-inch
- Addr Buffer

Memory Address Signal

Time [ns]

/1MA(20) : /1MA(19)
- design/B1U5-21./pinInst
- design/B0U5-34./pinInst
- design/B1U4-21./pinInst
- design/B1U3-21./pinInst
Write Data Waveforms @ SRAM Inputs

FPGA Addr Driver on Pulsar

9-inch

Bank0

FPGA Data Driver on Pulsar

9-inch

Bank1

Addr Buffer

Data Buffer

Memory Data Signal (Write)
Read Data Waveforms @Data Buffer Inputs

FPGA Addr Driver on Pulsar -> 9-inch -> Addr Buffer -> Bank0

FPGA Data Receiver on Pulsar -> 9-inch -> Bank1

Memory Data Signal (READ)

$V_{max}$ 3.3
$V_{inh}$
$V_{Meas}$ 1.8
$V_{Meas}$ 1.3
$V_{inl}$ 0.8
$V_{min}$ 0.00
$V_{min}$ -0.2

Time [ns]

/MD(11)
design/B0U3-31/pinInst
design/B1U3-24/pinInst
design/U19-5/pinInst
Read Data Waveforms @ FPGA Inputs

FPGA Addr Driver on Pulsar

9-inch

Addr Buffer

7-inch (inner layer)

FPGA Data Receiver on Pulsar

Data Buffer

---

Signal from Memory Buffer to FPGA over 7-in 50-ohms line

-Time [ns]

VINH 0.8

VIMH 0.0

VHmax 3.2

VMeas 1.6

VIML 0.4

VHmax 3.2

VMeas 1.6

VIML 0.4

/INNER_TRACE_7INS
design/I7INS-1./pinInst
design/I7INSL-1./pinInst
http://edg.uchicago.edu/~tang/Memory/sram_M4M.html