Memory Data Signal (Write)

- $V_{H_{\text{max}}}$
- $V_{\text{in}}$
- $V_{\text{Meas}}$
- $V_{\text{H}_{\text{max}}}$
- $V_{\text{L}_{\text{min}}}$

Time [ns]

/MD(11)

- red: design/B0U3-31./pinInst
- blue: design/U19-5./pinInst
- green: design/B1U3-24./pinInst
Signal from FPGA to Memory Buffer over 9-in 50-ohm line
Signal from Memory Buffer to FPGA over 7-in 50-ohms line
Driver FPGA (red), Receiver: ALVC162244 (blue), Line: 9in
47ohm/47p AC termination

/TOP_TRACE_9IN
design/T9INS-1./pinInst  design/T9INL-1./pinInst