Specifications for a common RAM mezzanine for the SVT upgrade
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1 Introduction

For the SVT upgrade we are going to implement in the Pulsar board several SVT functions. There will be Pulsar boards with the following three different kinds of firmware:

- AMS/RW
- HB
- TF

All these boards require extra RAM to implement the SVT functions listed above. In the following we describe the RAM requirement for those functions and define a common mezzanine card that satisfies the requirements of all boards.

2 RAM requirements

2.1 AMS/RW board

The AMS/RW board will require ISPY and OSPY memories that can be implemented using RAM on the Pulsar board. In addition the AMS/RW needs SSmap and AMmap memory.
SSmap is 128k x 12 bits (17 addr x 12 data).
AMmap is 1M x 36 bits (20 addr x 36 data).

2.2 HB board

The HB board will require ISPY and OSPY memories that can be implemented using RAM on the Pulsar board and a mezzanine card on the auxiliary board. In addition the HB needs SSmap, AMmap, HLM, and HCM memory.
SSmap is 128k x 12 bits (17 addr x 12 data).
AMmap is 1M x 36 bits (20 addr x 36 data).
HLM is 256k x 21 bits (18 addr x 21 data).
HCM is 32k x 4 bits (15 addr x 4 data).
The HCM will be contained in on-board Pulsar memory. The SSmap and AMmap will share a single 4Mx48-bit mezzanine card.

2.3 TF board

The TF board requires for each I/O FPGA (1) an SSmap that gives for every road the lower edge of the superstrip at each layer and (2) an intercept memory that provides 14 bits for each of three parameters using as the address the road number and a 3-bit hit map.
Intercept is 4M x 42 bits (22 addr x 42 data).
SSmap is 512k x 24 bits (19 addr x 24 data).

mezzanine	HB	AMS/RW	TF
RAM1	AMmap/SSmap	AMmap	intercept1
RAM2	HLM	SSmap	SSmap
RAM1	—	—	intercept2
RAM2	—	—	SSmap

Table 1: The use of RAM1-2 for a maximum of 4 mezzanine cards is shown for each board function (HB, AMS/RW, TF)

3 Mezzanine board

3.1 RAM blocks

Two single-width mezzanine boards can satisfy these requirements. The mezzanine cards are organized as follows:

- RAM1: 4M x 48 bits (22 addr x 48 data)
- RAM2: 512k x 24 bits (19 addr x 24 data)

Table 1 shows that the HB and AMS/RW will mount 2 mezzanine cards while the TF will mount 4 mezzanines cards. In addition, the HB will mount a RAM2 card on the auxiliary board for the OSPY memory.

3.2 CMC specifications

The pulsar board has four mezzanine card slots at the front of the board. Each slot has 2 CMC connectors providing up to 83 user defined signals directly visible to motherboard FPGAs. The mezzanine card connections are all bi-directional. The implementation follows CMC[1] standard (Common Mezzanine Card). The mezzanine should also follow the CMC standard.

3.3 IO specifications

The connector pin assignments are specified an an accompanying document.

3.4 RAM chip specifications

Memory chips satisfying these requirements are Cyprus CY7C1069AV33 and CY7C1012AV33.

References

[1] IEEE Computer Society. Draft standard for a common mezzanine card family: Cmc. IEEE P1386/Draft 2.0, 1995. 2