



CYPRESS

SRAM System Design Guidelines

Introduction

This application note examines some of the important system design considerations an engineer should keep in mind when designing with Cypress SRAMs. It is important to note that while they are not required, each guideline, if properly implemented, will lead to excellent long-term system performance. Moreover, they are simply smart electrical engineering practices.

The topics covered in this application note are decoupling capacitors, printed circuit board (PCB) issues, and terminations.

Decoupling (Bypass) Capacitors

Decoupling capacitors, also commonly referred to as bypass caps, are often the most confusing component in a high-speed digital design. Engineers know that capacitors need to be in the design, but the purpose and operation of the part is often unclear. Additionally, as the speed of signals increases, many older designs using the same decoupling methodology need to be updated.

Simply put, the reason systems need decoupling capacitors is to reduce the amount of noise in the power system. More specifically, the goal of this capacitor is to eliminate the effects of inductance on the power supply bus. Essentially, the capacitor, which has a low series resistance and series inductance, decouples or “bypasses” the power supply bus from the IC.

The decoupling capacitor has three major purposes. It is used to prevent voltage swing on the power and ground pins, it provides a low impedance path from the power plane to the ground plane, and it provides a signal return path between the power and ground planes.

The Problem with Inductance—Ground Bounce

An important function of the decoupling capacitor is to eliminate the effects of inductance. But why is inductance a big problem? To examine how big a problem the wiring inductance can be, consider *Equation 1* below.

$$V = \left(\frac{dI}{dt}\right) \times L \quad \text{Eq. 1}$$

This equation states that a change (or surge) in the current taken across a finite inductance will cause an increase in voltage. Generally, when an integrated circuit (IC) is behaving statically, the wiring inductance is not a problem. With the device’s outputs not switching, the current being drawn by the device does not change, and there is no additional voltage (noise) on the power lines.

When the outputs of the IC switch, however, there will be a surge in current as the IC attempts to drive its loads to a higher or lower voltage level. This surge in current may cause significant noise to be added to the power lines.

Consider *Figure 1* below, which shows the simplified schematic of an output of an SRAM. The inductors that are shown represent the wiring inductance between the die of the device and the power plane. The output goes to a high voltage level when transistor Q1 is on and transistor Q2 is off. The output is tied to ground and a low voltage level when Q2 is on and Q1 is off.

At the moment that Q2 turns on and Q1 turns off, there is a spike of current that flows from the output to the ground, through transistor Q2. This changing current also flows through the intrinsic and wiring inductance shown and according to *Equation 1* changes the voltage at Reference B. In other words, as Q2 turns on and the voltage at the output begins to drop, the voltage at Reference B (which, ideally, would be zero volts) will actually rise due to the current spike. Thus, the output voltage V_{OUT} does not fall all the way to zero like it should, but rather “bounces” above a grounded voltage level. This is what is known as *ground bounce*. A similar result will occur at Reference A when Q1 switches on and the current spike drives the output high. In this case, the ending value of V_{OUT} will be below V_{DD} , and we call the effect *voltage droop*.

Picking the Right Capacitor Value

To alleviate the problems of ground bounce and voltage drop, decoupling capacitors should be connected between each power pin on a device and ground. The initial capacitance value that is chosen is done to provide a minimum current need. When the output buffers of an SRAM switch, the power terminals will sag due to the effects described above. The function of the decoupling capacitor is to supply this momentary need in current with its stored charge. To do this, it must store a minimum amount of energy. The buffer loading determines this energy and the amount stored is given by the formula:

$$Q = CV \quad \text{Eq. 2}$$

where:
Q = charge stored
V = applied voltage
C = bypass capacitance in farads.

Differentiating this equation yields

$$I(t) = \frac{dQ}{dt} = C \times \frac{dV}{dt} \quad \text{Eq. 3}$$

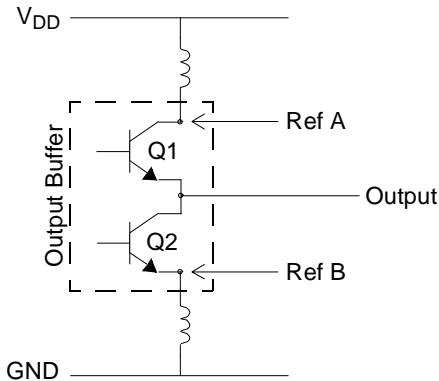


Figure 1. Effects of Ground Bounce

This equation allows us to calculate the capacitance required to prevent the voltage drops due to the switching output drivers. For example, suppose we have an SRAM with eighteen 3.3V output drivers driving a 50-ohm trace with a rise and fall time of 3 ns. Let us also assume that a voltage drop of 300 mV is the maximum amount of voltage drop allowable to the component.

First, we need to calculate the output current during the rise of the clocks. Assuming the outputs reach 3V, each output requires $3V/50 \text{ ohm} = 60 \text{ mA}$. Because the SRAM has eighteen such drivers, the total current required is 1080 mA.

Solving for C in Equation 3 above yields

$$C = I \times \frac{dt}{dV}$$

$$C = 1080\text{mA} \times \frac{3\text{ns}}{300\text{mV}} = 0.0108\mu\text{F} \quad \text{Eq. 4}$$

This suggests that this amount of total capacitance is required on the component to maintain less than 300 mV of voltage swing. Often, 0.1- μF capacitors are used for bypassing. Another way to view this situation is to say that a 0.1- μF capacitor supplies 1080 mA of instantaneous current in 3ns with only 32.4 mV of voltage swing across the bypass capacitor.

This example assumed a worst-case scenario voltage swing on the outputs of 3V. Depending on the termination method used, this swing could be less than this amount. However, since this is used only as a guide, it is best to overestimate the value.

Capacitor Filtering

We have seen that the main role of decoupling capacitors is to block unwanted noise going onto and coming from the power plane. It should be noted, however, that decoupling caps are much more than a capacitor. Since capacitors always have a finite, intrinsic resistance and inductance, they are, in effect, a capacitor in series with an inductor and a resistor, as shown in Figure 2 below.

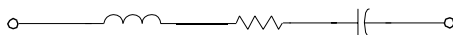


Figure 2. Capacitor Model

This is important in understanding what happens during the operation of a capacitor. Consider Figure 3, which shows the behavior of two ideal components, a capacitor and an inductor, which represent the reactive parts of the capacitor shown in Figure 2. Note that without any lead inductance or resistance, the resulting capacitive reactance approaches 0 Ω with increasing frequency. Note also that the inductive reactance of the ideal inductor, without any stray capacitance, approaches infinity.

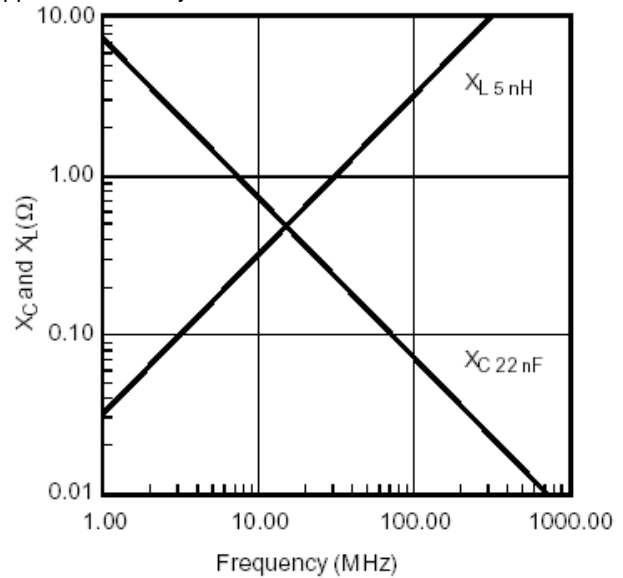


Figure 3. Z vs. f for Parts of a Real Capacitor

The impedance curve of “Real” capacitors resembles the traces marked 22 nF and 100 pF of Figure 4. The shape of these calculated curves match those found in a capacitor manufacturer’s data sheets. This means that, in a circuit, a capacitor acts as a low-impedance element only over a limited range of frequencies. To extend this frequency range, many references propose adding a second capacitor to bypass frequencies outside the limited range of the single capacitor. This approach expects a resulting impedance curve like the solid line marked “Expected” in Figure 4. This solution, however, is not mathematically sound and has a significant problem at “intermediate” frequencies.

What actually happens when two capacitors of different values are in parallel is shown in Figure 5. Notice the spike in impedance just above 100 MHz. The goal of obtaining lower impedance across a wider frequency is not achieved. On the contrary, the impedance has actually increased in some areas. Therefore, the practice of using two different valued capacitors to decouple a power supply bus is not recommended.

But, there is a method that will help to lower the impedance across all frequencies. When two capacitors of the same value and package size are in parallel with each other, no peak increase in impedance is realized. However, they do have the effect of halving the inductance. This is a recommended practice, however it may be constrained by available board space.

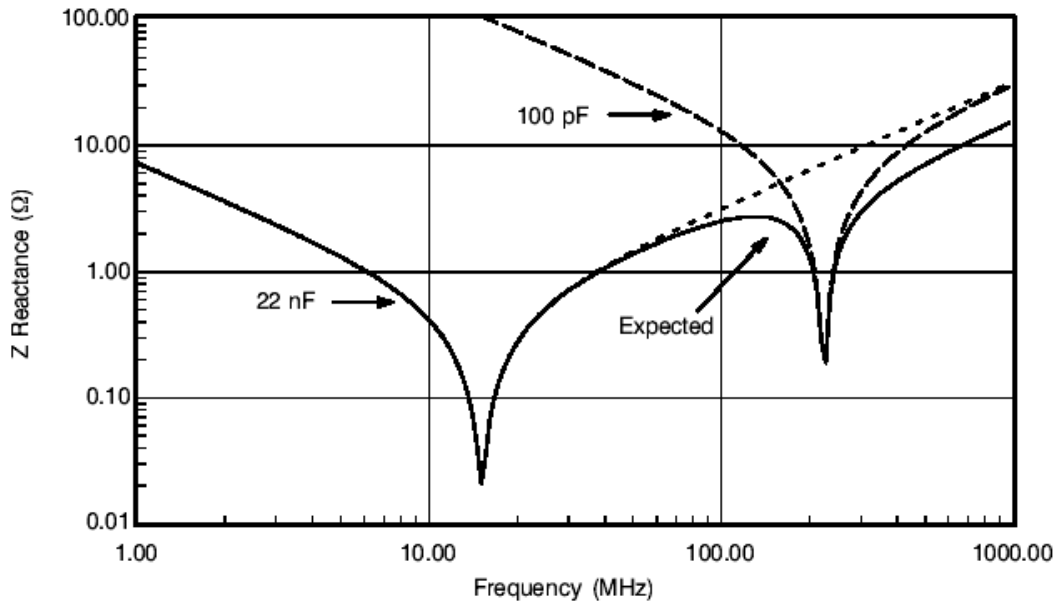


Figure 4. Expected Impedance of "Real" Capacitors

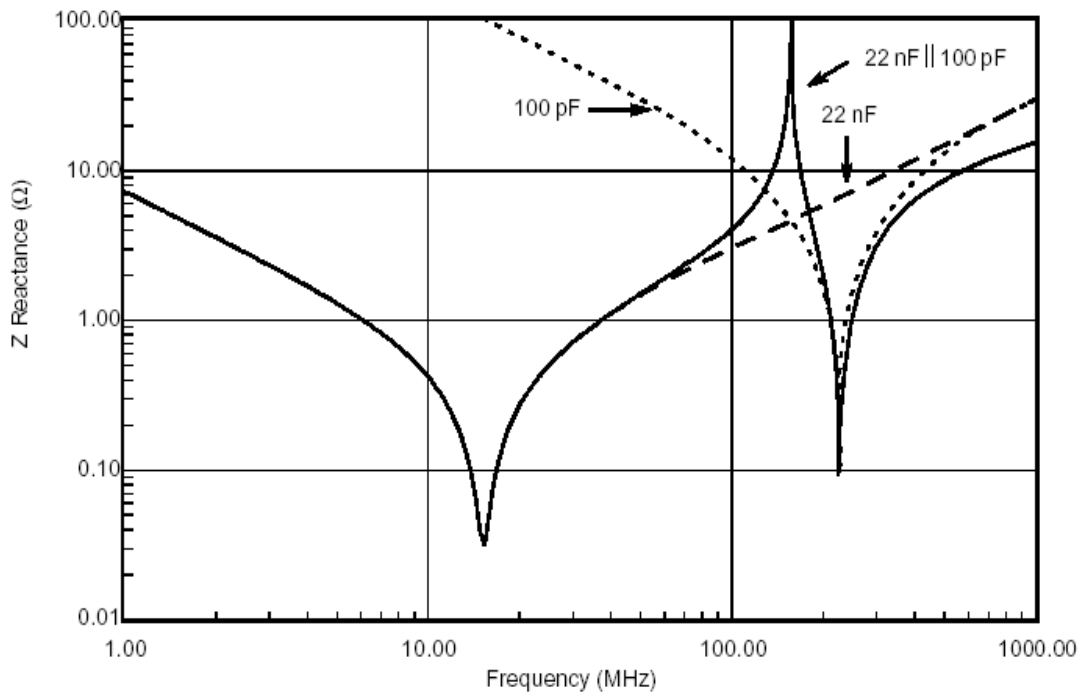


Figure 5. Real Z vs. f for Parallel 22-nF and 100-nF Capacitors

What Frequencies to Bypass

It is a common misconception that faster clock rates lead to the need for higher frequency decoupling. This is only partly true. Because the frequencies have increased, the technology for high-speed memories has been driven to provide faster rise and fall times. Therefore, a signal whose frequency is 1 MHz will need the same decoupling as a clock running at 50 MHz using the same high-speed buffers. The difference may be that there is more timing margin afforded in the slower speed system. A rough generalization suggests that frequencies up to one half the fastest signal transition rate (rise or fall) frequency need to be bypassed:

$$f_{BYPASS} = 0.5 / \text{Transition Rate.}$$

It should be noted that decoupling is really a four-part system comprising the power supply, bulk capacitors, decoupling capacitors, and intrinsic capacitance in the board. Each provides decoupling in its respective frequency bands with the power supply addressing the very low frequencies and the intrinsic board capacitance addressing the high frequencies. The difference between the capacitance is large enough between each part that the large spiking effect with multiple capacitor value interaction explained above does not occur. However, between each frequency band there will be small peaks. These peaks will always exist but they can be moved slightly.

Generally, engineers have limited ability to alter the characteristics of the power supply and board plane capacitance. But it is possible to vary the bulk and decoupling capacitance values. The goal is to have the four-part system provide a low impedance path (less than 1 ohm) throughout the frequency range. By adjusting the values of the decoupling capacitors, the small impedance peaks can be shifted to allow for the lowest impedance in the frequency ranges of concern.

Decoupling Capacitors: Design Recommendations

As we have now seen, decoupling capacitors play a huge role in how well the SRAM performs. Along with appropriately picking the right value capacitor, connecting them on the board is of extreme importance in terms of performance. Generally, a PCB should be designed to keep wiring and lead inductances as low as possible. Long, narrow PCB traces should be avoided because they increase inductance. Passing through a via is acceptable provided the path is lower inductance than an alternative longer trace. The following is a list of rules when designing with decoupling capacitors.

1. Use only one value capacitor for the component.
2. Keep decoupling capacitors as close to the component as possible.
3. Use a minimum of one capacitor on each power pin.
4. Keep capacitors on the same side of the board as the component, if possible.
5. Minimize the lead and wiring inductance.
6. Ensure that the capacitor value meets the voltage swing requirements, and that it provides a low-impedance path to ground in the intended frequency range of the application.

PCB Layout Considerations

The PCB provides two significant functions in an electrical design: mechanical locations for the components that reside on the board, and connectivity between components. These connections play an important role in providing a solid pathway to the power system and ensuring the highest degree of signal integrity.

The traces and planes that comprise a printed circuit board can be separated into two categories. There are pathways for the power source and there are traces required to carry the actual signals. This section of the application note will examine how both of these directly affect system integrity.

Power and Ground Planes

Power planes are large sheets of a conductive material that typically reside on entire PCB layers. They provide four primary functions to the circuit. They are:

1. a low-impedance path for power from its source to the components on the PCB.
2. a physical channel to vent and move heat from the components.
3. electrostatic shielding between the electromagnetic fields of signal traces that run on both sides of the planes.
4. a sheet capacitance for the ground plane that exists on other layers of the PCB. This in turn provides additional AC bypassing within the power circuitry of the PCB.

The primary functionality of a power plane is to reduce the resistance that causes a voltage drop between component and power source. The thickest power plane available will provide the best results. For example, using a two-ounce copper power plane instead of a one-ounce will cut in half any point-to-point path resistance. It can be thought of as having two resistors (and inductors) in parallel. The increased plane thickness reduces both the DC resistance and AC inductance drops. The drop in DC resistance allows the power supply to reach the component cleanly, while the reduction in AC inductance provides a low-impedance path for signal return currents.

As a secondary benefit, the thicker plane also increases the ability to sink heat out of the component. The bond wires and lead frames are a major thermal path in non-heat-sinked components.

The planes also aid in the reduction of electromagnetic interference (EMI). They provide a lower-impedance path across which the EMI develops and a larger faraday shield to short out these radiated fields.

The sheet capacitance that the power plane provides is proportional to its size, its distance from the ground plane, and the dielectric constant of the material between them. It has the benefit of providing bypass capacitance, particularly at the high frequencies. While it is far from being sufficient to provide all of the bypassing needs of a high-speed logic design, it should be utilized to its maximum. The capacitance of the planes can be calculated by the following equation:

$$C = 0.225E_R((N-1) \times A) / t \quad \text{Eq. 5}$$

where:

E_R = The relative dielectric constant

N = Number of plates

A = Area of one side of one plate in square inches

t = Thickness (separation of plates) in inches

For example, using a 10-inch by 10-inch FR-4 board with an E_R of 4.1 and 0.005-inch separation between the power and ground plane, the capacitance is calculated as

$$C = 0.225(4.1)((2-1) \times 100) / 0.005 = 18,450 \text{ pF} \quad \text{Eq. 6}$$

This is equivalent to 184 pF per square inch. *Table 1* shows the dielectric constants for several common materials used in PCB design today. It is always advisable to consult your fabricator for the precise E_R value, since different epoxies are used when constructing a PCB. Dielectric constants of PCBs also change with frequency, as shown in *Table 1*.

Table 1. Dielectric Constants

Material	E_R	
	@ 1 MHz	@ 300 MHz
FR-4, Tetra Functional	4.2 – 4.6	4.0 – 4.3
FR-4, High-grade Multifunctional	4.2 – 4.6	4.1 – 4.4
Polyimide	4.2 – 4.6	4.1 – 4.3
GETEK	3.9 – 4.1	3.9 – 4.0
BT	3.6 – 4.1	3.55 – 4.0
CE	3.6 – 4.0	3.6 – 4.0

Vias

Vias are commonly used to connect the power plane to the power traces that ultimately attach to the power pins of the components. They can also have an impact on the power signal quality.

First, vias produce a higher resistance than a copper trace. This is due to the material typically used in the fabrication of the via, which is plated granular copper. The resistance of a via changes based on the thickness of the copper that is plated in the via hole. Therefore, larger vias have a lower DC resistance and hence develop less of a DC voltage drop for any given current.

Vias also add inductance to the power trace. This inductance causes high-frequency noise that is present on the power plane to stay on the plane (which is good), but it also isolates the capacitance effect of the power plane from the components on the other ends of the vias. Filling vias with solder, using heavy plating, enlarging their size and using multiple vias per power connection are the preferred methods of lowering both the resistive and inductive parasitic effects they have on power connections.

Power Traces

Similar to vias, a trace also has some amount of resistance, capacitance, and inductance. The overall resistance must be kept to a minimum to avoid voltage drop on the trace. For the power plane to reach the power trace and ultimately the component, a via is also required.

If connections to the device are made in correct sequence, the resistance and inductance of the trace and via will isolate the component's noise from passing into the power plane.

This effect increases as the frequency of the noise rises. To achieve this isolation, the power trace must pass from the via to the decoupling capacitors pad and then to the component. This order is important to create an island of protected trace between the decoupling capacitor and the component.

It is important to highlight that the trace between component and bypass capacitor be as short as possible. As we have mentioned, the goal is to keep the inductance between the devices to a minimum. A short, wide trace will produce better results than a long, narrow trace.

Signal Return Paths

The power planes play a key role in the return currents of high-speed digital signals. At very slow speeds, the return current follows the path of least resistance. At higher speeds, however, the return currents follow the path of least inductance. This can be on either power or ground plane, directly below the signal trace. Normally, the return path is on the ground plane on standard PCB designs. When the return current reaches the driving component, the decoupling capacitors provide the bridge to the proper voltage plane.

In order to maintain good signal integrity and to minimize crosstalk, a clean, unobstructed return path needs to be provided. For example, if a return signal encounters a 5-ohm trace within the ground plane, the integrity of the normal signal on the 50-ohm trace can be compromised.

There are a few simple rules to follow for planes. First, it should be as continuous as possible. By placing excessive clearances around holes that pass through, it may make fabrication easier but it can cause the return current to travel through a non-optimal path. The effect of the clearance holes should be analyzed. Second, cutouts in the ground plane must be avoided. Similar to the clearance holes for the vias, a ground plane cutout will force the return path current around the cutout if the signal trace crosses above the cutout. This will increase the inductance of the path and decrease the rise time of the digital signal on the trace. It will also increase the potential for crosstalk.

Crosstalk

Crosstalk can exist between traces on a PCB. If this occurs on a memory signal with sufficiently strong amplitude, a false trigger can occur. Crosstalk should therefore be minimized in the design.

As a signal travels through a trace, it creates a magnetic field. It also reacts to other magnetic fields within its path. These magnetic fields have adverse effects on digital signals since they create unwanted noise on other signals. This effect is known as *crosstalk*. The voltages that external fields cause are proportional to the strength of the external fields and the length of the trace that is exposed to the field. Often, the trace that causes the crosstalk is termed the "source" or "aggressor," and the trace that is affected first is called the "victim."

Crosstalk between traces is a function of both mutual inductance and mutual capacitance. A model of inductance and capacitance between traces is shown in *Figure 6*. Its magnitude is proportional to the distance from the source trace, the speed of the signal edge rate, and the impedance of the victim trace. In digital systems, crosstalk caused by mutual inductance is typically equal to or larger than the crosstalk associated with mutual capacitance.

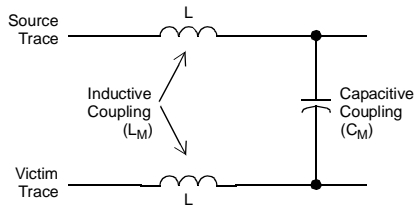


Figure 6. Mutual Coupling Between Traces

To illustrate the effects of spacing, the mutual inductance L_M can be calculated with the following equation:

$$L_M = \frac{L}{\left(1 + \left(\frac{s}{h}\right)^2\right)} \quad \text{Eq. 7}$$

where:
 L = Inductance of the wire
 s = separation between the wires
 h = height above the plane

This shows that moving the traces away (value s) from each other or by moving the traces closer (value h) to the plane, the mutual inductance is reduced by the square of the change. And, since crosstalk is proportional to the mutual inductance, the magnitude of the crosstalk is also reduced. *Figure 7* below illustrates this model.

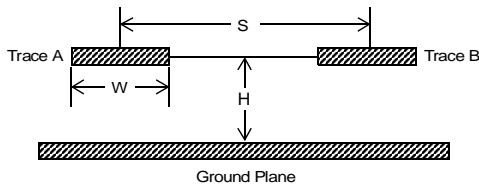


Figure 7. Trace and Ground Planes

The mutual capacitance C_M injects current I_M into the victim trace and can be calculated as:

$$I_M = C_M \times \frac{dV_s}{dt} \quad \text{Eq. 8}$$

where:
 $dV_s = V_s$ is the source voltage

Figure 8 illustrates the effects of trace impedance on crosstalk coupling. The higher the impedance of the victim trace, the more susceptible it is to noise from crosstalk. *Figure 9* shows a similar effect but with varying the width of the trace line. Wider traces produce less crosstalk coupling. Therefore, minimum coupling is created with maximum spacing, maximum trace widths, and minimum impedance.

To minimize the effects of magnetic field coupling, three basic rules should be followed.

First, separate the traces with more distance. The effect that is seen is directly proportional to the square of the distance of the elements and therefore doubling the distance will reduce the coupling by a factor of four.

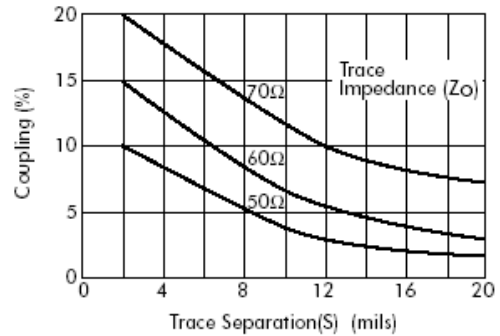


Figure 8. Crosstalk versus Impedance and Spacing

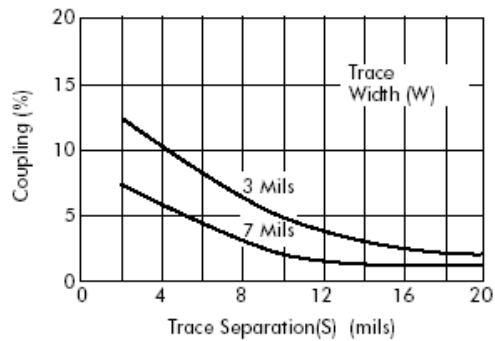


Figure 9. Crosstalk versus Width and Spacing

The second method of decreasing the coupling is to shield the target trace. Either routing it on another layer or placing protective guard traces between the two does this. In this way the magnetic lines will have a portion of their energy developed in the protective traces, usually at ground potential, and the field that cuts across the trace being shielded is less.

A third way to reduce the impact of crosstalk is to use differential signaling. This type of signal rejects noise from crosstalk if both true and complement signals are equally affected. This is commonly called common-mode noise rejection. However, if the crosstalk affects one trace of the differential pair and not the other, noise coupling can be a factor.

Layers

In order to keep noise at a minimum and to achieve the best in signal integrity, control of the PCB layers is required.

As was mentioned above, spacing power and ground planes close together gains additional bypassing capacitance. Of more importance is the creation of a reference plane that provides constant trace impedance. The reference plane is usually the ground plane. The thickness of the substrate between controlled impedance traces and the ground plane must be selected to be both manufacturable and able to keep the desired characteristic trace impedance within acceptable limits. As the spacing of layers decreases, the ability to hold tight, repeatable spacing value decreases. A 1-mil variation on a 10-mil spacing is 10% and on a 20-mil spacing it is only 5%. You should consult with your manufacturer on the tolerances.

When power planes are correctly bypassed, they are at the same AC potential as ground planes. Therefore, they can be used as a reference for controlled impedance traces. Using both power and ground planes, however, is unwise because the transition between the two has a high potential of causing noticeable impedance discontinuities in trace impedance, which is a source of unwanted reflections. (This application note will explain reflections in more detail in the next section.)

Vias in Traces

When routing a trace, the signal should remain on the same signal plan. Using a via to route to another plane diminishes signal quality. Vias should therefore be avoided as much as possible. If vias have to be used in a high-speed design, the following guidelines should be considered.

1. Make vias as large as possible (more area equals less inductance and resistance).
2. Plate external layers with the maximum thickness of copper during fabrication.
3. Plating of filling the via holes solid.

Reflections and Terminations

Another problem that arises in digital signal systems involves reflections due to poorly terminated transmission lines. This section will discuss a few important points to remember when designing with long wiring networks. For a full discussion on transmission lines, please refer to the Terminations application note available on the Cypress web site.

What is a Reflection?

A reflection is an unwanted pulse on a transmission line that is a result of an unmatched source or load impedance. The transmission line has an intrinsic value called its characteristic impedance. A reflection back toward the driver source can occur if the line's load and characteristic impedances are not matched, and a second reflection back toward the load can occur if the source and characteristic impedances are also not matched.

Why do Reflections Occur?

Reflections occur because of impedance mismatches that cause a disproportion of energy transfer. If the line is ideal, and the source impedance Z_S equals the load impedance Z_L , then half the energy in the propagating signal will be lost in the source impedance, and the other half in the load impedance (since the ideal line is lossless). However, if the load resistor at the end of the line is larger than the line's characteristic impedance, there will be extra energy available that is "reflected" back toward the source. That is, there is another signal that propagates down the line that "bounces" off the load if there is an impedance mismatch.

Characteristic Impedance

The most important variable of any line is its characteristic, or input, impedance. This is the impedance seen looking into the two left-hand terminals of the line.

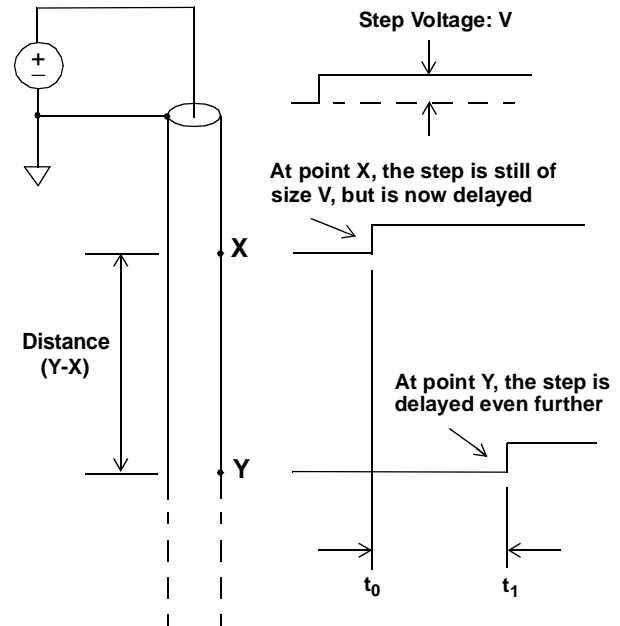


Figure 10. Voltage Step Input to an Ideal Line

Figure 10 below illustrates how a digital pulse propagates down an ideal line. The pulse is set onto the beginning of the line by the source at time $t = 0$. This pulse is then transferred down the line without being distorted or attenuated while it is delayed in time according to the line's propagation delay. At point X, the voltage on the line is low, until time t_0 at which time the signal passes point X on the line, and we can see that the pulse drives the voltage up to the high level. A similar situation exists for point Y, except that the signal stays low longer while it waits for the pulse to propagate down the line.

We can find the characteristic impedance of this line by finding the amount of current it takes to impress the step voltage on a given length of the line, in this case between arbitrary points Y and X.

The capacitance of the length of line between points X and Y is given as:

$$C_{xy} = \left(\frac{C}{in}\right) \times (Y-X) \quad . \quad \text{Eq. 9}$$

The total additional charge necessary to charge the capacitance between these points is equal to:

$$\text{Charge} = C_{xy} = \left(\frac{C}{in}\right)(Y-X)V \quad . \quad \text{Eq. 10}$$

The time interval (in seconds) in which during which C_{xy} must be charged is equal to the separation of the two points times the propagation delay in seconds per unit length:

$$T = (Y-X) \sqrt{\left(\frac{L}{in}\right) \left(\frac{C}{in}\right)} \quad . \quad \text{Eq. 11}$$

The average current supplied is equal to the total charge supplied divided by the length of time T:

$$I = \frac{\text{Charge}}{T} = \frac{\left(\frac{C}{\text{in}}\right)(Y-X)V}{(Y-X)\sqrt{\left(\frac{L}{\text{in}}\right)\left(\frac{C}{\text{in}}\right)}} \quad \text{Eq. 12}$$

This gives us the current flow required to sustain a propagating step edge of V volts. Therefore, the characteristic impedance of an ideal line can be found through simplification

$$Z_0 = \frac{V}{I} = \sqrt{\frac{L}{C}} \quad \text{Eq. 13}$$

where L and C are given in per-unit lengths.

As this equation shows, the value of characteristic impedance for ideal lines is real-valued, constant, and dependent only on the inductance and capacitance of the line-per-unit length. This allows us to model a transmission line as a simple resistor.

The characteristic impedance equation given above for an ideal line does not depend on the frequency of the system. This is not the case for a lossy line, however. The general formula for characteristic impedance is given as

$$Z_0 = \frac{V}{I} = \sqrt{\frac{R + j\omega L}{j\omega C}} \quad \text{Eq. 14}$$

This is the impedance if a finite value of resistance exists. Note that Z_0 is actually a function of frequency. However, since digital signals operate at very high frequency along PCB traces that have very low resistance, it is simpler to use the form given in *Equation 10*.

Termination Strategies

The end goal of all termination strategies is to remove voltage reflection on the line by cancelling out the two voltage reflection coefficients. There are two general strategies for doing this:

1. match the load impedance to the line's characteristic impedance.
2. match the source impedance to the line's characteristics impedance.

Under one of these conditions, the load or source reflection coefficient will be made to equal zero and thus there will be no reflection. If the load is matched, there will be no reflection back to the source, and if the source is matched, this reflection will not bounce back again toward the load. Matching the load is slightly preferred, since eliminating the first reflection will reduce EMI and electrical noise, and also it seems logical to try and eliminate any reflections as soon as one might occur.

approved kkv 10/_/02