The First Look of ps-Discriminator Design and Simulation

Fukun Tang 10/25/07

Schematic Diagram:

- **33.5db Limiting Amplifier**
- **11.5db Comparator/Line Driver**
- **MCP**
- **Threshold**
Input: A typical of 1mA current pulse with rise time of 1ns and fall time of 10ns.
Threshold: -10mv
Outputs (OUT+, OUT-): 700mv swing
Propagation Delay and Output Rise Time

Propagation Delay = 100ps (120ps to 1.2V CMOS Vt)

Tr = 60ps
Discriminator Outputs with Fixed Input, Multi-Threshold ($\Delta V_{th} = -10\text{mV}$)

It seems to be linear! Good!
Time Walk with 10X Overdriven Inputs (1mA-10mA)
Figure out the time walk by yourself
Disturbs on Threshold

2mV disturb on the threshold pin
Limiting Amplifier Schematic
Comparator Schematic

Substrate tie-down discussed later
Limiting Amplifier
Gain & Phase Characteristics

Active Gain = 33.5 dB

Gain & phase is simulated with signal-end input and differential outputs.

BW(-3db) = 3.1 GHz
ps-Discriminator (limiting amp + comparator)

Gain & Phase Characteristics

- **Gain & phase** is simulated with signal-end input and differential outputs.
- **Active Gain** = 45db
- **BW(-3db)** = 3.1Ghz
- **Gain**
- **Phase**

**Gain**
- M0(45.01dB)
- M1(41.99dB)

**Phase**
- OUT+
- OUT-
Equivalent Input Noise

- 1/f noise (<200Hz)
- Equivalent Input Noise: < 0.95 nV/√Hz @ 1K
POWER CONSUMPTION

+2.5V, 50mA    125mW
-1.2V, 30mA    60mW

Total Power = ~200mW
Substrate Tie-down Potential
---Homework on Gary’s question

- Power Supplies: +2.5V, +1.2V, -1.2V, DGND, AGND.

- Which voltage should substrate tie to? -1.2V or Ground?

Proposed VDDs and Logic Levels for CMOS gates:

1. 1.2V CMOS Logic:
   \[ VDD=1.2V, \quad \text{Logic Low} = 0V, \quad \text{Logic High} = 1.2V \]

2. 2.5V CMOS Logic:
   \[ VDD=2.5V, \quad \text{Logic Low} = 0V, \quad \text{Logic High} = 2.5V \]

3. Substrate Potential = 0.
In CMOS, the substrate should tie to the most negative voltage to prevent PN diodes formed by p-bulk and (S,D) from being forward biased. However, the CMOS threshold are significant affected by the substrate potential. The threshold will be increasing with the substrate tie-down potential goes down.

In IBM Reference Manual, all the CMOS test data are obtained by connecting substrate to GROUND.
From this cross section view, the substrate potential seems to be no affect to hetero-junction bipolar transistor, even the emitter connects to the negative voltage (-1.2V).
When NPN transistor is (deeply) saturated, the parasitic pnp will be conducted and feeds current into substrate, that causes substrate noise.