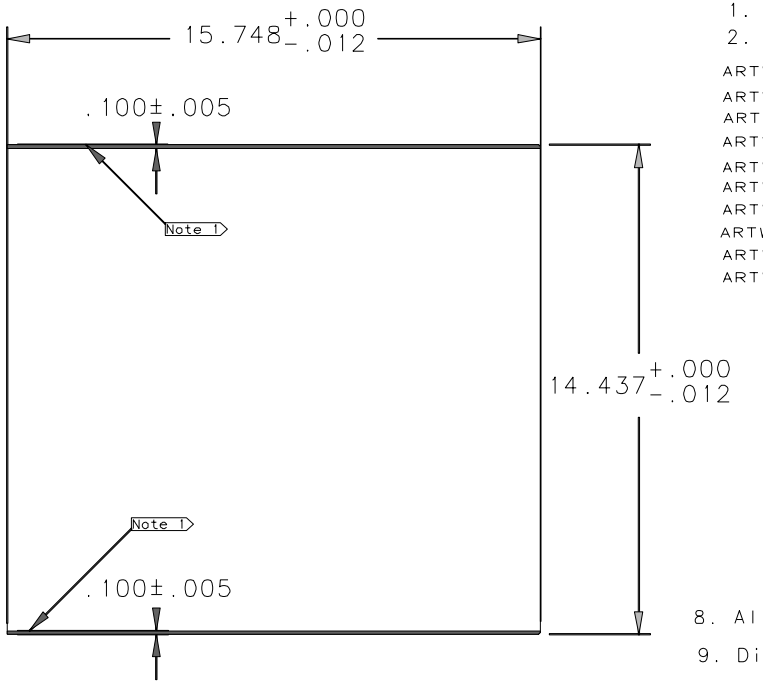

NOTE 1: Mill board solder side to a thickness of 0.062" +/- 0.008 along both edges shown in drawing
NOTE 2: Finished plated hole size, min 0.59mm, max 0.65mm

BOARD's DRILL SCHEDULE (Inch)

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.018	3842	YES	---
⊞	.02	39	YES	---
⊕	.0236	254	YES	---
⊟	.041	459	YES	---
⊖	.052	14	YES	---
◫	.106	7	NO	---
⊕	.113	6	NO	---
□	.16	1	YES	---

Note 2

B2536V1.0 PC BOARD SPECIFICATIONS

1. Board Layers: 10 (4 signal layers, 6 power layers)
2. Layer Stack Order:

ARTWORK_1: Top Component Layer (Signal_1, PAD_1)
ARTWORK_2: POWER PLANE VCC (POWER_1)
ARTWORK_3: POWER_PLANE GROUND (POWER_2)
ARTWORK_4: POWER PLANE VCC0, VCC1, P3V3, VEE (POWER_3, POWER_5, POWER_8, POWER_10)
ARTWORK_5: Inner Signal Layer (Signal_3)
ARTWORK_6: Inner Signal Layer (Signal_4)
ARTWORK_7: POWER PLANE AGND (POWE_7)
ARTWORK_8: POWER PLANE VEE0, VEE1, VINIT (POWER_4, POWER_6, POWER_9)
ARTWORK_9: POWER_PLANE GROUND (POWER_2)
ARTWORK_10: Solder Side Layer (Signal_2, PAD_2)

3. Apply solder mask over bare copper on both side:
   Artwork_11: Top component side solder mask.
   Artwork_12: Bottom component side solder mask.
4. Apply silkscreen on both side:
   Artwork_13: Top component side silkscreen.
   Artwork_14: Bottom component side silkscreen.
5. Solder paste photo plots
   Artwork_15: Top solder paste mask
   Artwork_16: Bottom csolder paste mask
6. Material: FR4 with Tg >170C.
7. Board thickness: 0.093'' +/- 0.010. see Note 1 for edge processing
8. All power layers use 1 oz copper, all signal layers uses 0.5 oz. before plating,
9. Differential trace impedance control at 90 ohms +/- 10%. Trace/gap = 7/7 mils
10. All single ended traces impedance should be matched on all layers
11. Min trace, clearence = 7 mils
12. Ni/Au (chem plated) over bare copper.
13. Apply solder mask over bare copper
14. Send back photo plots and layer stack parameters for rechecking.
15. All dimensions are in inches unless otherwise noted.

16: Contact person:
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SCM# B2535 V1.0
SPC# B2336 V1.0
ASM# B2337 V1.0

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
B2536 Specification Drawing

SHEET 1 OF 1
DATE 1-5-2004
DRAWN F. Tang

B– 2536
REV 1.0