B2545V1.0 PC BOARD SPECIFICATIONS

1. Board Layers: 4
2. Layer Stack Order:
   ARTWORK_1: Top Component Layer (Signal_1, PAD_1)
   ARTWORK_2: Power Plane Ground (POWER_1)
   ARTWORK_3: Power Plane Ground (POWER_1)
   ARTWORK_4: Solder Side Layer (Signal_2, PAD_2)

3. Apply silkscreen on both side:
   Artwork_5: Top component side silkscreen.
   Artwork_6: Bottom component side silkscreen.

4. Apply solder mask over bare copper on both side:
   Artwork_7: Top component side solder mask.
   Artwork_8: Bottom component side solder mask.

5. Solder paste photo plots
   Artwork_9: Top solder paste mask
   Artwork_10: Bottom solder paste mask

6. Material: FR4 with Tg >170°C.
7. Board thickness: 0.070" +/- 0.010.
8. All power layers use 1 oz copper, all signal layers use 0.5 oz. before plating.
9. Differential trace impedance control at 90 ohms +/- 10%. Trace/gap = 7/7 mils.
10. All single ended traces impedance should be matched on all layers.
11. Minimum trace, clearance = 7 mils.
12. Ni/Au (chem plated) over bare copper.
13. Apply solder mask over bare copper.
14. Send back photo plots and layer stack parameters for rechecking.
15. All dimensions are in inches unless otherwise noted.

BOARD's DRILL SCHEDULE (Inch)

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<th>DRILL SYMBOL</th>
<th>DRILL SIZE</th>
<th>COUNT</th>
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<th>Min/Max</th>
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NOTE: Pressfit hole, finished plated hole size, min 0.59mm max 0.65mm

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SCM# B2544 V1.0
SPC# B2345 V1.0
ASM# B2346 V1.0

UNIVERSITY OF CHICAGO ELECTRONICS DEVELOPMENT GROUP
TITLE
B2545 Specification Drawing
SHEET 1 OF 1
DATE 3-9-2004
DRAWN F. Tang
REV 1.0