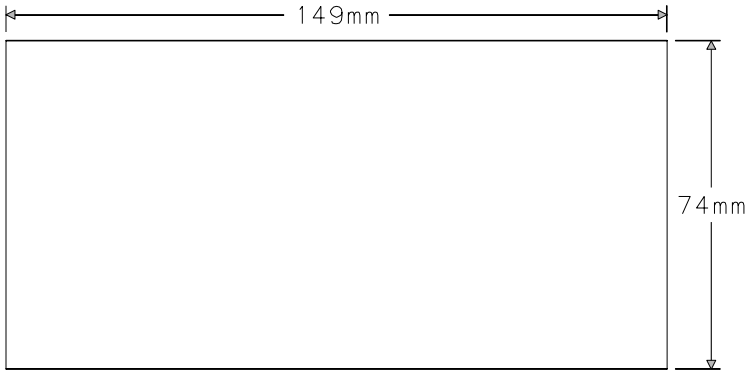
B2527 BOARD SPECIFICATIONS



1. Board Layers: 6
2. Layer Stack Order:

Layer1 (Artwork_1):	Top component layer (Signal_1), 1oz, Z(diff)=100 ohm
Layer2 (Artwork_2):	Power_4 (GROUND), 1oz
Layer3 (Artwork_3):	Power_2/POWER_3 (P2V5/P1V8), 1oz
Layer4 (Artwork_4):	Power_1 (P3V3), 1oz
Layer5 (Artwork_5):	Power_4 (GROUND), 1oz
Layer6 (Artwork_6):	Bottom component layer (signal_2), 1oz, Z(diff)=100 ohm

3. Apply silkscreen on both side:
   Artwork_7: Top silkscreen.
   Artwork_8: Bottom silkscreen
4. Apply solder mask over bare copper on both side:
   Artwork_9: Top solder mask
   Artwork_10: Bottom solde mask
5. Material: FR4
6. Board thickness: 0.062'' +/- 0.010.
7. Send me layer thickness specification for impedance varification
8. Copper thickness 1oz before plating for all the power planes.
9. Copper thickness 1oz before plating for all the signal layers.
10. Ni/Au plating (3 to 8 micro-inches soft gold) over bare copper
11. Differential pairs: trance width/gap=7/7 mils
12. All differential pairs impedance Z(diff) controlled at 100 ohm (+/-10%)
13. All other traces mininum clearance = 7 mils
14. All dimensions are in inches unless otherwise noted.

BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.013	40	YES	---
⊞	.015	290	YES	---
⌀	.02	26	YES	---
⊟	.035	2	YES	---
⊖	.037	18	YES	---
⊡	.041	50	YES	---
⊕	.055	2	YES	---
□	.062	4	YES	---
	.1063	5	YES	---

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SPC# B2527
ASM# B2528

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
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SHEET 1 OF 1
DATE 07/20/2003
DRAWN TANG

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