

B2555 BOARD SPECIFICATIONS

1. Board Layers: 8
2. Layer Stack Order:

Layer1 (Artwork_1): Top component layer (Signal_1), 1oz, Z=50 ohm
 Layer2 (Artwork_2): Power_1 (VCC), 2oz
 Layer3 (Artwork_3): Inner Layer, Signal_3, 1oz, Z=50 ohm
 Layer4 (Artwork_4): Power_2 (GROUND), 2oz
 Layer5 (Artwork_5): Power_1 (VCC), 2oz
 Layer6 (Artwork_6): Inner layer, Signal_4, 1oz, Z=50 ohm
 Layer7 (Artwork_7): Power_2 (GROUND), 2oz
 Layer8 (Artwork_8): Bottom component layer (signal_2), 1oz, Z=50 ohm

3. Apply silkscreen on both side:

Artwork_9: Top silkscreen.
 Artwork_10: Bottom silkscreen

4. Apply solder mask over bare copper on both side:

Artwork_11: Top solder mask
 Artwork_12: Bottom solde mask

5. Material: FR4
6. Board thickness: 0.062'' +/- 0.010.
7. Send me layer thickness specification for impedance varification
8. Copper thickness 2oz before plating for all the power planes.
9. Copper thickness 1oz before plating for all the signal layers.
10. Ni/Au plating (3 to 8 micro-inches soft gold) over bare copper
11. Trace width/gap=5/5 mils
12. All 5 mill trace impedance are controlled at 50 ohm +/-10%
- 13: All dimensions are in inches unless otherwise noted.

BOARD'S DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.01	885	YES	---
⊞	.02	19	YES	---
⊕	.041	10	YES	---
⊞	.055	4	YES	---
⊖	.1063	6	YES	---

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UNIVERSITY OF CHICAGO
 ELECTRONICS DEVELOPMENT GROUP

TITLE

B2555 specifications

SHEET 1 OF 1
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 DRAWN TANG

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