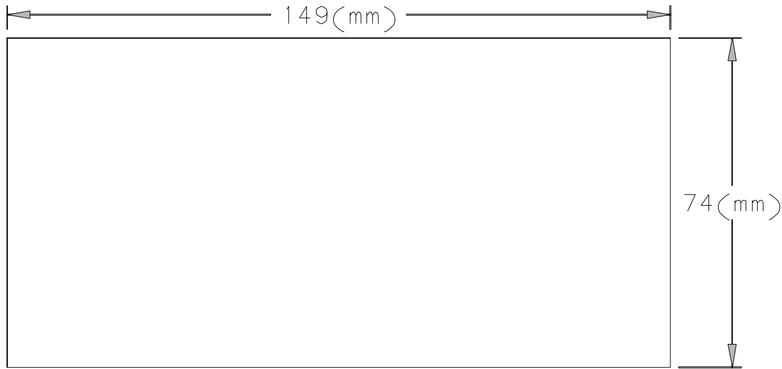

B2558 BOARD SPECIFICATIONS

1. Board Layers: 4

2. Layer Stack Order:

Layer1 (Artwork_1): Top component layer (Signal_1), 1oz, Z=50 ohm
Layer2 (Artwork_2): Power_1 (VCC), 1oz
Layer3 (Artwork_3): Power_2 (GROUND), 1oz
Layer4(Artwork_4): Bottom component layer (signal_2), 1oz, Z=50 ohm

3. Apply silkscreen on both side:
   Artwork_5: Top silkscreen.
   Artwork_6: Bottom silkscreen

4. Apply solder mask over bare copper on both side:
   Artwork_7: Top solder mask
   Artwork_8: Bottom solde mask

5. Material: FR4
6. Board thickness: 0.062'' +/- 0.010.
7. Send me layer thickness specification for impedance varification
8. Copper thickness 1oz before plating for all layers.
9. Ni/Au plating (3 to 8 micro-inches soft gold) over bare copper
10. Trace width/gap=5/5 mils
11. All 5 mill trace impedance are controlled at 50 ohm +/-10%
12: All dimensions are in inches unless otherwise noted.

BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.01	353	YES	---
⊞	.02	5	YES	---
⦶	.041	8	YES	---
⊟	.055	4	YES	---
⊖	.1063	8	YES	---

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SCH# B2557
SPC# B2558
ASM# B2559

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
B2558 specifications

SHEET 1 OF 1
DATE 2/17/2005
DRAWN TANG

B- 2558
REV 1.0