Schematic Drawing: C-2374
Assembly Drawing: C-2376

Board Origin

14.437 +.012
4.724 +.012

Note 45 degree chamfer.

Board Characteristics:
2. Board Thickness: 0.062" +/- 0.008" (2.36 +/- 0.2mm).
3. Minimum Trace Width 0.008" on all layers.
4. Minimum Clearance 0.008" on all layers.
5. 1 oz Copper for all Trace and Power Layers.
6. Apply Solder Mask over bare copper;
   exposed areas covered with solder.
7. Silkscreen on Both Sides
8. Interlayer spacing : as specified.
9. All hole diameter tolerances : +/- 0.002" unless specified.

AUX Card Drill Schedule (inches)

<table>
<thead>
<tr>
<th>THS</th>
<th>COUNT</th>
<th>PLATED</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>.02</td>
<td>1006</td>
<td>YES</td>
<td></td>
</tr>
<tr>
<td>.0236</td>
<td>379</td>
<td>YES</td>
<td>Note 10.</td>
</tr>
<tr>
<td>.024</td>
<td>143</td>
<td>YES</td>
<td></td>
</tr>
<tr>
<td>.033</td>
<td>300</td>
<td>YES</td>
<td></td>
</tr>
<tr>
<td>.041</td>
<td>179</td>
<td>YES</td>
<td></td>
</tr>
<tr>
<td>.052</td>
<td>2</td>
<td>YES</td>
<td></td>
</tr>
<tr>
<td>.057</td>
<td>2</td>
<td>YES</td>
<td></td>
</tr>
<tr>
<td>.106</td>
<td>24</td>
<td>YES</td>
<td></td>
</tr>
<tr>
<td>.113</td>
<td>6</td>
<td>NO</td>
<td></td>
</tr>
</tbody>
</table>

Note 10: This is a pressfit technology through hole tin plated
with the following specification:
10-1. Finished hole size: 0.6mm +/- 0.05mm
10-2. Drilled hole size: 0.7mm +/- 0.02mm
10-3. Thickness of Copper plating: min 25 µm Cu
10-4. Thickness of tin plating: 5-15 µm Sn.

Layer Order:
1. Signal 1
2. Power 1 (+5v)
3. Signal 2
4. Signal 3
5. Power 2 (gnd)
6. Signal 4

CERN CDF L1 Auxiliary Board Specification Drawing

Contact Info:

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APPROVALS:

ENRICO FERMILAB INST., UNIV. OF CHICAGO
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INSTRUMENTATION

SCALE 1/2