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CrateSum Functional Document

Upgrade for Run II

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1 Introduction and Overview

The upgraded Level 1 calorimetry trigger planned for Run II will be entirely digital, deadtimeless and designed to accommodate shorter bunch spacings, higher trigger bandwidth and the plug upgrade [1, 2]. This note describes the purpose and functionality of the new CrateSum (CS) board within the context of this new system. Detailed information on the design and hardware implementation of this board can be found in Reference [3].

The role of each calorimetry trigger crate will be the same as in Run I [4], except that it will only be used in Level 1 (L1). See Figures 1 and 2 for a schematic of the system and the crate layout. Each crate will calculate $\sum^{\mathrm{Wedge}} \mathrm{E_T}$ for each of four wedges. ($\sum^{\mathrm{Wedge}} \mathrm{E_T}$ is the transverse energy summed over all η for both Hadronic (Had) and Electromagnetic (EM) calorimeters in one 15 degree wedge in the azimuthal angle ϕ.) Each crate will also use tracking to help determine how many trigger towers pass various triggers. The standard CDF upgrade crate setup [5] includes two CrateSum[1] boards and sixteen Digital Information Receive and Compare (DIRAC) boards [6] within each crate. Each DIRAC uses calorimetry tower energy and tracking information to decide which towers pass a given trigger. DIRAC also sums up the total energy deposited in its towers above a given threshold. Both results are passed to a CrateSum board along a custom backplane. CrateSum uses information from eight (consisting of two sets of four) DIRACs to summarize the triggers passed and to compute the total energy deposited in each of the two groups of four boards. These results are carried by front panel connectors to a PreFRED module [7] in the Global Level 1 crate and used to make a L1 decision.

2 Level 1 Calorimetry Crate Functional Description

2.1 The Standard CDF VME Crate and Backplanes

The standard CDF upgrade crate is a 9U VME crate and contains a Motorola MVME2301 VMEbus Readout Controller (VRC) and a **TR**igger **A**nd **C**lock + **E**vent **R**eadout

[1] In the upgrade, it's really a "Half-Crate" Sum.

(TRACER) Module [8] to interface with the DAQ system and the Trigger Supervisor Interface (TSI)[2]. Further information about the TSI can be found in Reference [9].

There are two backplanes in the readout crate. The upper backplane is a CDF standard backplane and has three connectors for each slot. These are P1, P0, and P2, listing them in order from the top to bottom. (The associated backplane segments are called J1, J0, and J2, respectively.) P1 is the standard 5-row VME-P P1 [10] connector with 32 pins in each row. P0 is a power connection that is not used by CrateSum. P2 is a connector with five rows of pins. The middle row of pins on P2 are for standard VME signals and the two rows on either side are reserved for global CDF control signals. For CrateSum, these rows are used to pass the TSI control signals from the TRACER module. The outermost two rows are defined in the VME64 Extensions Draft Standard [11].

The second backplane, J3, has been custom-built to pass point-to-point signals between DIRAC and CrateSum and is described in detail in [12]. The boards are placed as shown in Figure 2. Note that each CrateSum receives signals from eight DIRACs, four on each side. Each set of four DIRACs on each side of CrateSum receives signals from an entire ϕ wedge ($-3.51 \leq \eta \leq 3.51$ for both Had and EM).

2.2 DIRAC

The overall data flow chart for the L1 calorimetry crate is shown in Figure 3. The $\eta - \phi$ map for both the physical and trigger towers has changed from that used in Run 1 [13]. Each DIRAC will now take in 12 trigger towers with the same ϕ, half from the Had calorimeter and half from the EM. For each tower, DIRAC reads in 10 bits of $\mathrm{E_T}$ data from the Front-End with 0.125 GeV least count and 128 GeV full scale[3]. This information is used in conjunction with the tracking information from the XFT to determine how many towers, if any, on the board satisfy each of a number of triggers. The results are stored as a 16-bit word which consists of ten 1-bit trigger results (pass/nopass) and three 2-bit trigger results (0, 1, 2 or $\geq$ 2 trigger towers passing). In addition, DIRAC forms an 8-bit $\overset{\mathrm{DIRAC}}{\Sigma}\ \mathrm{E_T}$ word with 0.50 GeV least count and 128 GeV full scale for all towers above some shoulder $\mathrm{E_T}$ value. These two summaries from one DIRAC card are placed on the J3 backplane along with the results from seven other DIRAC cards and passed to the appropriate CrateSum board. Note that the energy summing on DIRAC occurs before the tracking information arrives, and can be passed on to CrateSum before the trigger summary is completed. Thus, the energy summing and trigger summary sections work independently. For further discussion of DIRAC, see Reference [6].

[2]The VRC, TSI, and the TRACER will be referred to as the DAQ when VME interactions are under discussion. Although the VRC and the TRACER modules are both involved in passing on control signals from the TSI to CrateSum, such communications initiated or received by the TSI will simply be referred to as being made with the TSI without mention of the VRC and TRACER.

[3]Note that the scale is the same as that used in run 1A [14] and is imposed in order to both keep the number of output bits per board to a minimum as well as to keep a large full scale. Note also that placing limitations on the full scale range and energy resolution of the L1 trigger may have consequences for future physics uses.

2.3 CrateSum

Since the $\overset{\text{DIRAC}}{\Sigma}\ \mathrm{E_T}$ and trigger words from the DIRAC cards may be available at different times, CrateSum begins the process of making an energy or trigger summary by latching either the eight trigger words or eight $\overset{\text{DIRAC}}{\Sigma}\ \mathrm{E_T}$ words on the J3 backplane at independently adjustable times. CrateSum receives the $\mathrm{E_T}$ information for all calorimeter towers from two different ϕ wedges (four DIRACs per wedge and two sets of four DIRACs), so it produces $\overset{\text{Wedge}}{\Sigma}\ \mathrm{E_T}$ for each wedge. Each of these two 10-bit summaries indicates an $\mathrm{E_T}$ between 0 and 512 GeV with 0.5 GeV least count. If the 8-bit word from any DIRAC has all bits set, all bits are turned on in the 10-bit CrateSum $\mathrm{E_T}$ summary for that wedge.

On the trigger front, CrateSum has the capability to use the eight 16-bit DIRAC trigger words it receives to produce a maximum 20-bit half-crate summary consisting of any combination of 1-bit, 2-bit, or 3-bit words adding up to a total of 20 bits. The current trigger summary algorithm involves producing a 1-bit sum for each of bits 0 to 9 from each of the DIRAC boards and 2-bit sums for DIRAC bits 10 to 15. In other words, CrateSum's bit X trigger sum ($X \in \{0,1,2,3,4,5,6,7,8,9\}$) is the logical .OR. of the trigger bits X coming from each of eight DIRAC boards, CrateSum's output bits 11 and 10 are the sum of DIRAC bits 11 and 10, and the same relationships hold between CrateSum bits 13 and 12 and DIRAC bits 13 and 12 and between CrateSum bits 15 and 14 and DIRAC bits 15 and 14. CrateSum trigger bits (19:16) are spare bits and currently set to 0. Table 1 shows how the CrateSum trigger bits are formed from DIRAC trigger bits.

CrateSum Output Trigger Bits

CrateSum Trigger Bits	Are formed from DIRAC bit(s):
TRIG(19:16)	*Spare bits*
TRIG(15:14)	(15:14)
TRIG(13:12)	(13:12)
TRIG(11:10)	(11:10)
TRIG(9)	(9)
TRIG(8)	(8)
TRIG(7)	(7)
TRIG(6)	(6)
TRIG(5)	(5)
TRIG(4)	(4)
TRIG(3)	(3)
TRIG(2)	(2)
TRIG(1)	(1)
TRIG(0)	(0)

Table 1: Labels for the CrateSum trigger bit summaries.

The use of programmable logic devices (PLDs) permits flexibility in specifying the summary algorithms. Both the $\mathrm{E_T}$ and trigger processing programs are implemented in a single large PLD. This allows the trigger summary algorithm, in particular, to be changed should such a change be deemed necessary.

The E_T and trigger summaries are latched into FIFOs and are also sent to the PreFRED modules to be processed for use in the Global Level 1 crate in making a L1 decision. Also stored in FIFOs are the bunch number of the event and the original eight $\overset{\text{DIRAC}}{\Sigma} E_T$ words and eight DIRAC trigger summaries. Storage of both DIRAC and CrateSum energy and trigger summaries on CrateSum is controlled by TSI signals on the J2 backplane. These summaries can be read out by the DAQ in the event of a Level 2 accept (L2A).

3 CrateSum Input and Output Connectors

The front panel and backplane connectors and their functions are summarized in Table 2.

Connector	Description
CS-FR1	Front panel connector used to send out energy signals from CS to PreFRED.
CS-FR2	Front panel connector used to send out trigger signals from CS to PreFRED.
CS-P1	VME J1 backplane connector. Passes VME instructions and data.
CS-P2	VME J2 backplane connector. Used for VME and TSI interactions.
CS-P3	Custom J3 backplane connector. Passes DIRAC $\overset{\text{DIRAC}}{\Sigma} E_T$ and trigger data to CS.

Table 2: List of CrateSum front panel and backplane connectors. Note that the P0 connector on the backplane is not used by CrateSum.

3.1 Front Panel Connectors

CrateSum has two front panel connectors[4], labeled CS-FR1 and CS-FR2, which deliver the two wedge energy and trigger summaries, respectively, to the Aux-cards [12] in the Global Level 1 crate. The Aux-cards translate the differential input data signals into individual signals directly usable by PreFRED and also place these bits on the custom backplane where they are available to PreFRED.

Table 3 lists the signals output from CS-FR1 and CS-FR2. For the purposes of this document, “Wedge 0” will refer to the ϕ wedge represented by the set of four DIRACs to the immediate left of the CS board when looking at the VME crate face-on. In other words, this is the set of DIRAC boards with smaller slot numbers than CrateSum. “Wedge 1” will refer to the set on the right (larger slot numbers). Note that this definition of the wedges is NOT that used in the PreFRED specification [7].

The CS-FR1 connector sends out the two 10-bit $\overset{\text{Wedge}}{\Sigma} E_T$ words, one for each wedge, in two sequential steps of 66 ns each, on the same data lines[5]. PreFRED requires CrateSum to send out either the Wedge 0 or Wedge 1 $\overset{\text{Wedge}}{\Sigma} E_T$ word first, depending on the location (crate

[4] 20-pin SCSI-II type connectors are used.

[5] This procedure halves the number of required lines, thus allowing the use of 20-pin connectors rather than the high-density 40-pin ones originally considered.

Signal Name	Description
ET_PHI0(9)	Most Significant Bit, $\overset{\text{Wedge}}{\Sigma}\ \mathrm{E_T}$ 0th wedge
ET_PHI0(8)	Next to Most Significant Bit, $\overset{\text{Wedge}}{\Sigma}\ \mathrm{E_T}$ 0th wedge
⋮	⋮
ET_PHI0(1)	Next to Least Significant Bit, $\overset{\text{Wedge}}{\Sigma}\ \mathrm{E_T}$ 0th wedge
ET_PHI0(0)	Least Significant Bit, $\overset{\text{Wedge}}{\Sigma}\ \mathrm{E_T}$ 0th wedge
ET_PHI1(9)	Most Significant Bit, $\overset{\text{Wedge}}{\Sigma}\ \mathrm{E_T}$ 1st wedge
ET_PHI1(8)	Next to Most Significant Bit, $\overset{\text{Wedge}}{\Sigma}\ \mathrm{E_T}$ 1st wedge
⋮	⋮
ET_PHI1(1)	Next to Least Significant Bit, $\overset{\text{Wedge}}{\Sigma}\ \mathrm{E_T}$ 1st wedge
ET_PHI1(0)	Least Significant Bit, $\overset{\text{Wedge}}{\Sigma}\ \mathrm{E_T}$ 1st wedge
TRIG(19)	Trigger Bit 19
TRIG(18)	Trigger Bit 18
⋮	⋮
TRIG(1)	Trigger Bit 1
TRIG(0)	Trigger Bit 0

Table 3: CrateSum output signal names. "Wedge 0" corresponds to the set of four DIRACs to the left of a particular CrateSum board and "Wedge 1" to the four boards to the right.

and slot number) of the particular CrateSum board involved. Please refer to the PreFRED specification [7] for details. The status of a "parity" register on CrateSum indicates which wedge energy summary is output first. If the value of this bit is 0, the Wedge 0 $\mathrm{E_T}$ word is returned first, and then Wedge 1. If the value is 1, Wedge 1 is output first, and subsequently, Wedge 0. The value of the "parity" bit must be downloaded before the beginning of a run. The CS-FR2 connector likewise sends out the trigger bit summary in two sequential words. The three double-bit trigger bits are sent in the first 66 ns and the ten single-bit trigger bits in the subsequent 66 ns. To prevent data corruption and decrease noise, differential signals are used to pass data from CrateSum to the Global Level 1 crate. Tables 4 and 5 list the pin assignments for the CS-FR1 and CS-FR2 connectors.

3.2 Backplane Connectors

CS-P1, CS-P2, and CS-P3 are the backplane connectors and connect to the J1, J2, and J3 backplanes, respectively. They are used for downloading, run-time interactions with the TSI, readout, diagnostics, and for receiving data from DIRAC. CS-P1 and CS-P2 are standard VMEbus connectors which are VME64 extension compatible. The user-defined pins on CS-P2 provide additional power and ground beyond the VME standard, as well as pass along

Pin	Signal, Cycle 1	Pin	Signal, Cycle 1	Pin	Signal, Cycle 2	Pin	Signal, Cycle 2
1	ET_PHIA(0)	2	$\overline{\text{ET\_PHIA(0)}}$	1	ET_PHIB(0)	2	$\overline{\text{ET\_PHIB(0)}}$
3	ET_PHIA(1)	4	$\overline{\text{ET\_PHIA(1)}}$	3	ET_PHIB(1)	4	$\overline{\text{ET\_PHIB(1)}}$
5	ET_PHIA(2)	6	$\overline{\text{ET\_PHIA(2)}}$	5	ET_PHIB(2)	6	$\overline{\text{ET\_PHIB(2)}}$
7	ET_PHIA(3)	8	$\overline{\text{ET\_PHIA(3)}}$	7	ET_PHIB(3)	8	$\overline{\text{ET\_PHIB(3)}}$
9	ET_PHIA(4)	10	$\overline{\text{ET\_PHIA(4)}}$	9	ET_PHIB(4)	10	$\overline{\text{ET\_PHIB(4)}}$
11	ET_PHIA(5)	12	$\overline{\text{ET\_PHIA(5)}}$	11	ET_PHIB(5)	12	$\overline{\text{ET\_PHIB(5)}}$
13	ET_PHIA(6)	14	$\overline{\text{ET\_PHIA(6)}}$	13	ET_PHIB(6)	14	$\overline{\text{ET\_PHIB(6)}}$
15	ET_PHIA(7)	16	$\overline{\text{ET\_PHIA(7)}}$	15	ET_PHIB(7)	16	$\overline{\text{ET\_PHIB(7)}}$
17	ET_PHIA(8)	18	$\overline{\text{ET\_PHIA(8)}}$	17	ET_PHIB(8)	18	$\overline{\text{ET\_PHIB(8)}}$
19	ET_PHIA(9)	20	$\overline{\text{ET\_PHIA(9)}}$	19	ET_PHIB(9)	20	$\overline{\text{ET\_PHIB(9)}}$

Table 4: Pin assignments for CS-FR1. Cycle 1 refers to the first 66 ns interval of a data cycle, and Cycle 2 refers to the second. A is 0 or 1 and B is 1 or 0 depending on the state of the "parity" register. If the value of this bit is 0, A is 0 and B is 1; if the value is 1, A is 1 and B is 0. The even-numbered pins are logical complements of the previous odd-numbered pins.

Pin	Signal, Cycle 1	Pin	Signal, Cycle 1	Pin	Signal, Cycle 2	Pin	Signal, Cycle 2
1	TRIG(10)	2	$\overline{\text{TRIG(10)}}$	1	TRIG(0)	2	$\overline{\text{TRIG(0)}}$
3	TRIG(11)	4	$\overline{\text{TRIG(11)}}$	3	TRIG(1)	4	$\overline{\text{TRIG(1)}}$
5	TRIG(12)	6	$\overline{\text{TRIG(12)}}$	5	TRIG(2)	6	$\overline{\text{TRIG(2)}}$
7	TRIG(13)	8	$\overline{\text{TRIG(13)}}$	7	TRIG(3)	8	$\overline{\text{TRIG(3)}}$
9	TRIG(14)	10	$\overline{\text{TRIG(14)}}$	9	TRIG(4)	10	$\overline{\text{TRIG(4)}}$
11	TRIG(15)	12	$\overline{\text{TRIG(15)}}$	11	TRIG(5)	12	$\overline{\text{TRIG(5)}}$
13	TRIG(16)	14	$\overline{\text{TRIG(16)}}$	13	TRIG(6)	14	$\overline{\text{TRIG(6)}}$
15	TRIG(17)	16	$\overline{\text{TRIG(17)}}$	15	TRIG(7)	16	$\overline{\text{TRIG(7)}}$
17	TRIG(18)	18	$\overline{\text{TRIG(18)}}$	17	TRIG(8)	18	$\overline{\text{TRIG(8)}}$
19	TRIG(19)	20	$\overline{\text{TRIG(19)}}$	19	TRIG(9)	20	$\overline{\text{TRIG(9)}}$

Table 5: Pin assignments for CS-FR2. Cycle 1 refers to the first 66 ns interval of a data cycle, and Cycle 2 refers to the second. TRIG(15) through TRIG(10) are the three 2-bit trigger bits and TRIG(9) through TRIG(0) are the ten single-bit trigger bits. TRIG(19) through TRIG(15) are spare bits.

signals from the TSI. Table 11 at the end of this document lists the signals controlled by the TSI. The small subset of signals used directly by CrateSum appears in boldface. Table 12 shows the pin connections for CS-P2. The CS-P3 connector[6] receives energy and trigger data from the eight DIRAC boards serviced by CrateSum. Table 13 lists the data bits from DIRAC and Table 14 lists the pin assignments on CS-P3. Note that if a DIRAC is not plugged in, CrateSum considers the input from that card to consist of all zeroes.

4 Run-time Dynamics

4.1 Start-up Sequence

To begin data-taking or to resume a run after a hardware error has been detected in the trigger system, the TSI/TRACER issue a sequence of signals to synchronize the L1 calorimeter trigger cards. This procedure involves the "HALT...RECOVER...RUN" sequence [15]. First the HALT signal (active low) is sent. When CrateSum receives this signal, it stops all clocking of data on the board, including all FIFO write and read operations and latching of data on the board. CrateSum then waits for the RECOVER signal (active low). On receipt of this signal, CrateSum resets its FIFOs, including the Bunch Counter FIFO. At the end of the recover cycle, the TSI sends a RUN signal which causes the TRACER to drop the HALT line. This tells CrateSum to prepare for data-taking. When the first BO signal is received after the deassertion of HALT[7], internal bunch and CDF_CLK counting is initiated on CrateSum. After a specific number of CDF_CLK cycles have passed, 132ns-period latching of DIRAC data into CrateSum can commence.

4.2 Dataflow

4.2.1 Clocking Data Through CrateSum

During the following discussion, reference will be made to several different sections of the CrateSum board. A functional schematic of the dataflow appears as Figure 4.

The flow of data on CrateSum is regulated by a number of 132ns-period clock signals output by the Controller PLD chip in the **CONTROL** block. Data is latched into the **P3_Latch** section at times $T_{\mathrm{P3\_Latch\_ET}}$ and $T_{\mathrm{P3\_Latch\_Trig}}$ after B0 to capture the energy and trigger bit information from the CS-P3 connector. Separate signals are sent for each since the energy and trigger summaries may arrive at different times and be from different events. However, it is assumed that all eight DIRAC summaries are available at the CS-P3 connector simultaneously. After the data has been latched in, it then becomes available for processing. The next few paragraphs describe the dynamics of processing the data and clocking it through the remainder of the board.

The half-crate energy summary is performed by two identical subsections in **Energy Summary**. Each of these subsections receives the four 8-bit $\overset{\mathrm{DIRAC}}{\Sigma}\mathrm{E_T}$ words from a single ϕ

[6]CS-P3 is a 220-pin 2mm hard metric (e.g. AMP Z-pack) connector with 5 columns of 44 pins each.

[7]The TSI guarantees that the RUN signal will be sent no fewer than 35 CDF_CLK cycles before the next B0 signal.

wedge and sums them into a single 10-bit word, $\overset{\text{Wedge}}{\Sigma}\,\mathrm{E_T}$. The **Trigger Summary** takes in the eight 16-bit trigger summaries from the **P3_Latch** and performs the 20-bit[8] half-crate summary. After the energy and trigger bit summaries are completed, they are latched. The latching clock signals (which are perhaps more properly to be regarded as "strobes") begin at times $\Delta T_{\mathrm{proc\_latch\_ET}}$ for the energy summary and $\Delta T_{\mathrm{proc\_latch\_Trig}}$ for the trigger bit summary. These times are defined relative to the times $T_{\mathrm{P3\_Latch\_ET}}$ and $T_{\mathrm{P3\_Latch\_Trig}}$, respectively. This will also be true for all other "ΔT"s in this discussion: i.e. If we let T_{x} denote the absolute time that the data processing action labeled by "x" occurs, then $\Delta T_{\mathrm{x}} \equiv T_{\mathrm{x}}$ - $T_{\mathrm{P3\_Latch\_ET}}$ if ΔT_{x} is related to energy processing and $\Delta T_{\mathrm{x}} \equiv T_{\mathrm{x}}$ - $T_{\mathrm{P3\_Latch\_Trig}}$ if ΔT_{x} is related to trigger bit processing. The energy and trigger bit summary and latching are performed by an Altera FLEX10K70 PLD.

Destination PreFRED

After being latched in the Processor chip, the summarized data is sent along two separate paths. One of these routes leads to PreFRED in the Global Level 1 Decision Crate. The 20-bit energy and trigger summaries are multiplexed internally in the Processor, which sends each summary in two parts of 10 bits, spaced by 66ns, to the front panel output drivers. The 132ns-period switching signals (one for energy data and one for trigger) are issued by the Controller, which times it to coincide with the summarized data latching strobes. This is done to maximize the time that the output multiplexed data is valid.

The three 2-bit trigger sums are sent in the first 66ns of a cycle, followed by the ten 1-bit trigger sums. The order of the Wedge 0 and Wedge 1 $\overset{\text{Wedge}}{\Sigma}\,\mathrm{E_T}$ data is determined by the parity register bit, which the Controller uses to adjust the polarity of the switching signal for the energy data multiplexer in the Processor.

Datastream Readout Path

After being latched, the summary data in the Processor is sent along another route that may result in its being read out over VME. See Figure 5. The data must be stored until it is either discarded or read out into the datastream. This is done in the two-stage process shown in Figure 5. The latched half-crate energy and trigger data are clocked into FIFOs starting at times $\Delta T_{\mathrm{L1FIFO\_ET\_Sum}}$ and $\Delta T_{\mathrm{L1FIFO\_Trig\_Sum}}$. The first data into each empty FIFO chip is immediately available at the FIFO's output registers. At some later time, the board will begin to receive L1 Decision signals from the TSI. If an event is accepted by the Level 1 trigger (L1A), the data for that event will be FIRST stored in a buffer (since the data is already available at the output registers of the appropriate FIFOs), and THEN the FIFOs will be strobed to place the data for the next event at their outputs, in anticipation of the next L1 decision. Data is stored in one of four buffer locations. Each L1A command is accompanied by a pair of signals (L2B0 and L2B1) indicating which of the buffer locations to store the data in. Later on, if L2 rejects the event, no buffer readout instruction is sent

[8]Currently, only 16 of these bits have been defined. The upper 4 bits are spare bits and are set to 0 at this time.

and the buffer can be overwritten on a subsequent L1A[9]. If a Level 1 Reject (L1R) signal is received for an event, data for the next event will be clocked onto the output registers of the FIFOs, overwriting the data of the L1-rejected event.[10]

It is not only CrateSum's summarized $\overset{\text{Wedge}}{\Sigma}\ \mathrm{E_T}$ and trigger data that are stored in FIFOs and buffers. Beginning at times $\Delta T_{\text{L1FIFO\_ET\_Raw}}$ and $\Delta T_{\text{L1FIFO\_Trig\_Raw}}$, the raw DIRAC $\overset{\text{DIRAC}}{\Sigma}\ \mathrm{E_T}$ and trigger bit words received by CrateSum on the backplane are clocked into FIFOs. This data is stored into buffers or clocked out and not stored, depending on the receipt of L1A or L1R signals, exactly like for CrateSum's summaries.

$T_{\text{P3\_Latch\_ET}}$ and $T_{\text{P3\_Latch\_Trig}}$

Only the times $T_{\text{P3\_Latch\_ET}}$ and $T_{\text{P3\_Latch\_Trig}}$ need to be downloaded before a run begins. The Controller chip has a bank of registers for the purpose of storing this, and other, information. Table 6 lists each register and its access mode type and VME address. These registers will be discussed in detail in the remainder of this document.

[9]Note that CrateSum does not keep track of which buffers are full, nor the results of any decision. If the TSI tells CrateSum to put an event in a given buffer, CS simply assumes that that buffer is free for writing.

[10]Note that since the energy and trigger summaries come at different times, latching the data into the FIFO occurs at different times. However, only a single clock out is required since the summaries are aligned by the FIFO.

CrateSum Control Registers

Word[bit]	Name	Access	VME Address	Description
0[5:0]	B0_offset_ET[5:0]	R/W	0x000000	Bunch 0 E_T offset in 132ns units
1[5:0]	B0_offset_Trig[5:0]	R/W	0x000004	Bunch 0 Trig offset in 132ns units
2[2:0]	DIRAC_ET_delay[2:0]	R/W	0x000008	Fine delay in increments of 22ns to latch in E_T data from P3
2[5:3]	DIRAC_Trig_delay[2:0]	R/W	"	Fine delay in increments of 22ns to latch in Trig data from P3
3[0]	run	R/W	0x00000C	Mode of operation: 1=run; 0=load
3[1]	recover	R/W	"	When asserted (=1) in load mode, resets the L1FIFOs and the board error bit
3[2]	FIFO_Rclk	R/W	"	When set to 1 in load mode, generates a strobe that reads out the L1FIFOs
3[3]	L2B_W	R/W	"	When set to 1 in load mode, generates a strobe to write to a DAQ buffer
3[5:4]	L2B[1:0]	R/W	"	In load mode, the DAQ buffer address to write to when L1B_W is asserted
4[7:0]	Mask_DIRAC[7:0]	R/W	0x000010	DIRAC masking bits
5[1:0]	ET_Sum_FF_Mask[1:0]	R/W	0x000014	E_T Sum Full FIFO flag masks
5[3:2]	Trig_Sum_FF_Mask[1:0]	R/W	"	Trig Sum Full FIFO flag masks
5[7:4]	ET_Raw_FF_Mask[3:0]	R/W	"	E_T Raw Full FIFO flag masks
6[7:0]	Trig_Raw_FF_Mask[7:0]	R/W	0x000018	Trig Raw Full FIFO flag masks
7[1:0]	FF_ET_Sum[1:0]	RO	0x00001C	E_T Sum Full FIFO flags
7[3:2]	FF_Trig_Sum[1:0]	RO	"	Trig Sum Full FIFO flags
7[7:4]	FF_ET_Raw[3:0]	RO	"	E_T Raw Full FIFO flags
8[7:0]	FF_Trig_Raw[7:0]	RO	0x000020	Trig Raw Full FIFO flags
9[1:0]	EF_ET_Sum[1:0]	RO	0x000024	E_T Sum Empty FIFO flags
9[3:2]	EF_Trig_Sum[1:0]	RO	"	Trig Sum Empty FIFO flags
9[7:4]	EF_ET_Raw[3:0]	RO	"	E_T Raw Empty FIFO flags
10[7:0]	EF_Trig_Raw[7:0]	RO	0x000028	Trig Raw Empty FIFO flags
11[0]	_P3_Latch_OE/src_data	R/W	0x00002C	When =0, P3_Latch is enabled and data is from P3; when =1, P3_Latch is disabled and data is fake VME data.
11[2]	Bunch_Ctr_FF_Mask	R/W	"	Bunch Counter Full FIFO flag mask
12[0]	proc_latch_clk_ET	R/W	0x000030	When set to 1 in load mode, generates a strobe that that enables the Processor to latch processed E_T data
12[1]	L1FIFO_Wclk_ET_Sum	R/W	"	When set to 1 in load mode, generates a strobe to latch data into the E_T Sum L1FIFOs
12[2]	proc_latch_clk_Trig	R/W	"	When set to 1 in load mode, generates a strobe that that enables the Processor to latch processed Trig data
12[3]	L1FIFO_Wclk_Trig_Sum	R/W	"	When set to 1 in load mode, generates a strobe to latch data into the Trig Sum L1FIFOs
12[4]	P3_Latch_clk_ET	R/W	"	When set to 1 in load mode, allows P3 Latch to latch DIRAC E_T data from P3
12[5]	P3_Latch_clk_Trig	R/W	"	When set to 1 in load mode, allows P3 Latch to latch DIRAC Trig data from P3
12[6]	L1FIFO_Wclk_ET_Raw	R/W	"	When set to 1 in load mode, generates a strobe to latch data into the E_T Raw L1FIFOs
12[7]	L1FIFO_Wclk_Trig_Raw	R/W	"	When set to 1 in load mode, generates a strobe to latch data into the Trig Raw L1FIFOs
13[0]	parity	R/W	0x000034	When =0, Wedge 0 E_T summary is output first on FP; when =1, Wedge 1 output first
13[1]	board_error	RO	"	Board error bit; is set when any Full FIFO flag is set, unless the flag is masked
13[2]	FF_Bunch_Ctr	RO	"	Bunch Counter Full FIFO flag
13[3]	EF_Bunch_Ctr	RO	"	Bunch Counter Empty FIFO flag
14[7]	src_config	RO	0x000038	Source configuring the FLEX10K devices: 0 = EPROMS; 1 = download cable
14[6:0]	ctrl_version[6:0]	RO	"	Controller version number
15[7:0]	proc_version[7:0]	RO	0x00003C	Processor version number

Table 6: CrateSum control registers. These are 8-bit words which map the 8 MSB of the VME 32-bit data bus. Bits which have no function specified can be used as spare bits.

The B0_offset_ET(5:0) register, a 6-bit register, stores the number of 132ns CDF_CLK cycles after the receipt of the B0 signal before CrateSum gets valid E_T data for the first event ("Bunch 0") from DIRAC on the P3 backplane. (The hardware allows this number to be any integer value between 1 and 64, although the number determined at the conclusion of system integration will be less than 41.) Likewise, the B0_offset_Trig(5:0) register stores the number of 132ns CDF_CLK cycles after B0 before CrateSum gets trigger data from DIRAC on P3.

CrateSum tap-delays the CDF_CLK signal it receives into 6 individual clock lines (CDF_CLK(5:0)), each consecutive line delayed by an incrementing multiple of 22ns, beginning with zero. The DIRAC_ET_delay(2:0) 3-bit register picks one of these 6 clock signals. The time $T_{\mathrm{P3\_Latch\_ET}}$ is then determined as the rising edge of the CDF_CLK(5:0) signal specified by DIRAC_ET_delay(2:0) in the particular CDF_CLK cycle indicated by B0_offset_ET(5:0). In other words, E_T data from P3 is latched on the rising edge of the CDF_CLK(5:0) clock (picked by DIRAC_ET_delay(2:0)) in the 132ns-period CDF_CLK multiple (indicated in B0_offset_ET(2:0)). The DIRAC_Trig_delay(2:0) register serves the same purpose for trigger data as DIRAC_ET_delay(2:0) does for E_T.

One can think of the B0_offset_ET(Trig) register as a coarse adjustment knob for the time $T_{\mathrm{P3\_Latch\_ET}}$ ($T_{\mathrm{P3\_Latch\_Trig}}$), in units of 132ns, after the assertion of B0. The DIRAC_ET(Trig)_delay is a fine adjustment tuning knob for this time.

As previously stated, only the times $T_{\mathrm{P3\_Latch\_ET}}$ and $T_{\mathrm{P3\_Latch\_Trig}}$ need to be downloaded before a run begins. To emphasize this point, although at the considerable risk of incurring the annoyance of the reader, it is stated here that $\Delta T_{\mathrm{proc\_latch\_ET}}$, $\Delta T_{\mathrm{L1FIFO\_ET\_Sum}}$, and $\Delta T_{\mathrm{L1FIFO\_ET\_Raw}}$, as well as the corresponding "ΔT"s for the trigger data, are not stored in downloadable registers. Their values are all "fixed" in the internal programmable logic of the Controller Altera PLD, and have been selected to allow sufficient time for data to be summarized (in the case of $\Delta T_{\mathrm{proc\_latch\_ET}}$), and for raw and summed data to be valid at the inputs of the appropriate L1FIFOs (for $\Delta T_{\mathrm{L1FIFO\_ET\_Sum}}$ and $\Delta T_{\mathrm{L1FIFO\_ET\_Raw}}$, respectively). These times are based on the 22ns-delayed CDF_CLK(5:0) signals. Table 7 shows the approximate values of these times.

ΔT Values

Name	Approximate Value in ns
$\Delta T_{\mathrm{L1FIFO\_ET\_Raw}}$	44
$\Delta T_{\mathrm{proc\_latch\_ET}}$	96
$\Delta T_{\mathrm{L1FIFO\_ET\_Sum}}$	110
$\Delta T_{\mathrm{L1FIFO\_Trig\_Raw}}$	44
$\Delta T_{\mathrm{proc\_latch\_Trig}}$	96
$\Delta T_{\mathrm{L1FIFO\_Trig\_Sum}}$	110

Table 7: The values of the various ΔTs for clocking data through CrateSum.

4.2.2 Datastream Readout

All data transferable via VME is associated with an address that serves as a handle for data write or read requests.[11] The VME address map for CrateSum appears as Table 8. The contents of L2 Buffers 0, 1, 2, and 3 are accessible via the "block" (VME Address bus bits (23:20)) addresses 8, 9, A, and B, respectively.

VME Address Map for CrateSum

Name	Port location	Access	VME Address (A23:A0)	Description
Control registers	Control	R/W	0x00003C:0x000000	
Module ID	Control	RO	0x10007C:0x100000	Module ID ASCII word
E_T data from VME	Control/Processor	WO	0x200000 0x200004	Wedge 0 Wedge 1
Trig data from VME	Control/Processor	WO	0x300000 0x300004 0x300008 0x30000C	Quarter 1 Quarter 2 Quarter 3 Quarter 4
Processor readout via VME	Processor	RO	0x400000 0x400004 0x400008 0x40000C 0x400010 0x400014 0x400018 0x40001C	ET_Raw Wedge 0 ET_Raw Wedge 1 Trig_Raw Quarter 1 Trig_Raw Quarter 2 Trig_Raw Quarter 3 Trig_Raw Quarter 4 ET_Sum Trig_Sum
Bunch Counter value from VME	Controller	WO	0x500000	
L2 Buffer 0	DAQ Buffer 0	RO	0x800020: 0x800000	See Table 9
L2 Buffer 1	DAQ Buffer 1	RO	0x900020: 0x900000	"
L2 Buffer 2	DAQ Buffer 2	RO	0xA00020: 0xA00000	"
L2 Buffer 3	DAQ Buffer 3	RO	0xB00020: 0xB00000	"

Table 8: VME address map for CrateSum. A1 and A0 are both zero because CDF uses full 32-bit (quad word) data transfers. VME Address bits (31:24) depend on the location of the board in the crate.

If an event is accepted by L2 (L2A), its data stored in buffers may be read out via VME transfers. There are two L2A datastream readout modes. In the normal mode, only the two 10-bit energy summaries for the two wedges and the 20-bit trigger summary are read out over VME. In the trigger diagnostic readout mode, the original 8-bit $\overset{\text{DIRAC}}{\Sigma}\, E_T$ and 16-bit trigger summary words from each DIRAC are also read out after the CrateSum energy and trigger summary results. In either mode,[12] all words can be readout in a single block transfer. Table 9 describes the structure and order of the words that can be read out into the datastream.

In the standard VME crate, only 32-bit VMEbus addressing and data transfers will be

[11] This 32-bit address is unique within a physical crate. The upper five bits of the address (bits (31:27)) specify the geographical address, more commonly known by its moniker 'slot number'. VME Address bits (26:24) are unused and set to 0. Since only 32-bit (quad byte) transfers are used, bits (1:0) are ignored and may be considered to be 0. If a particular CrateSum board is the target of a VME data transfer, it uses VME Address bits (23:2) to determine the data or location requested.

[12] There is a third "readout" mode, of course, namely that none of the data from CrateSum or DIRAC is read out into the datastream. DIRAC and CrateSum currently are not expected to provide the event data which are written to tape when events are accepted by the entire trigger system.

Datastream Readout Words

Word Number	Name	VME Address	Meaning of bits
0	Board Header	0x♠00000	Board Type: ‘000001010’ (9), Board Serial Number (10), Slot Number / GA (5), Bunch Counter Value (8)
1	E_T Summary	0x♠00004	Unused (12), $\overset{\text{Wedge1}}{\Sigma} E_T$ (10), $\overset{\text{Wedge0}}{\Sigma} E_T$ (10)
2	Trigger Summary	0x♠00008	Unused (12), ‘0000’ (4), 3 2-bit sums (6), 10 1-bit sums (10)
3	DIRAC E_T Wedge 0	0x♠0000C	$\overset{\text{DIRAC3}}{\Sigma} E_T$ (8), $\overset{\text{DIRAC2}}{\Sigma} E_T$ (8), $\overset{\text{DIRAC1}}{\Sigma} E_T$ (8), $\overset{\text{DIRAC0}}{\Sigma} E_T$ (8)
4	DIRAC E_T Wedge 1	0x♠00010	$\overset{\text{DIRAC7}}{\Sigma} E_T$ (8), $\overset{\text{DIRAC6}}{\Sigma} E_T$ (8), $\overset{\text{DIRAC5}}{\Sigma} E_T$ (8), $\overset{\text{DIRAC4}}{\Sigma} E_T$ (8)
5	DIRAC Trigger Bits Qtr 1	0x♠00014	DIRAC1 Trigger Bits (16), DIRAC0 Trigger Bits (16)
6	DIRAC Trigger Bits Qtr 2	0x♠00018	DIRAC3 Trigger Bits (16), DIRAC2 Trigger Bits (16)
7	DIRAC Trigger Bits Qtr 3	0x♠0001C	DIRAC5 Trigger Bits (16), DIRAC4 Trigger Bits (16)
8	DIRAC Trigger Bits Qtr 4	0x♠00020	DIRAC7 Trigger Bits (16), DIRAC6 Trigger Bits (16)

Table 9: Possible CrateSum readout words. The numbers in parentheses indicate the number of bits of the data immediately preceding it. The VME data bus is 32 bits wide, so each word in the table has a total of 32 bits. ♠ is a “wildcard” representing hex 8, 9, A, or B, depending on which buffer location the readout is from: whether 0, 1, 2, or 3, respectively. See Table 8.

used. The two single-wedge energy summaries are grouped as one word and the trigger summary as a separate word. Both words are read out in a single block transfer while in normal readout mode. These words are followed by the $\overset{\text{DIRAC}}{\Sigma} E_T$ data and trigger bits from DIRAC in the case of trigger diagnostic readout. The first word of the datastream is the board header word, which reports the bunch counter value of the event, the board serial number, and the board type. See [16] for details.

4.3 Downloading

The values of all writeable registers should be downloaded to CrateSum before the start of data-taking. CrateSum has two complementary operational modes: load and run. Before any other register can be written to, the board must be placed in load mode by writing a ‘0’ to the ‘run’ register bit. The words containing registers that require downloading are listed in Table 10. Note that although some registers in these words are strobe generators for diagnostics and are unrelated to run-time operations, the fact that only whole words can be accessed requires that they be de facto downloaded with null (‘0’) values. Moreover, although the initial values of all strobe registers are ‘0’ upon board power-up, as desired, they should be all be downloaded with ‘0’s to be sure of this.

Downloading and most diagnostics require the board to be in the load mode. Since downloading of all writeable registers is required upon board start-up and before beginning a run, the Controller has been designed to start up in the load mode. This feature has been incorporated in the design, not to obviate the need to download the operational mode bit at start-up (since the state of writeable registers should never be assumed without having previously written to them), but rather as a precaution in the event that this mode bit is not downloaded before attempting to write to other registers.

Registers Requiring Downloading

Word[bit]	Name	VME Address	Value to download (in binary)
0[5:0]	B0_offset_ET[5:0]	0x000000	Bunch 0 E_T offset in 132ns units
1[5:0]	B0_offset_Trig[5:0]	0x000004	Bunch 0 Trig offset in 132ns units
2[2:0]	DIRAC_ET_delay[2:0]	0x000008	Fine delay in increments of 22ns to latch in E_T data from P3
2[5:3]	DIRAC_Trig_delay[2:0]	"	Fine delay in increments of 22ns to latch in Trig data from P3
3[0]	run	0x00000C	0 initially; 1 after all other registers have been downloaded
3[1]	recover	"	0
3[2]	FIFO_Rclk	"	0
3[3]	L2B_W	"	0
3[5:4]	L2B[1:0]	"	00
4[7:0]	Mask_DIRAC[7:0]	0x000010	00000000 if no DIRACS are to be masked
5[1:0]	ET_Sum_FF_Mask[1:0]	0X000014	00 if no E_T Sum FIFOs need to be masked
5[3:2]	Trig_Sum_FF_Mask[1:0]	"	00 if no Trig Sum FIFOs need to be masked
5[7:4]	ET_Raw_FF_Mask[3:0]	"	0000 if no E_T Raw FIFOs need to be masked
6[7:0]	Trig_Raw_FF_Mask[7:0]	0x000018	00000000 if no Trig Raw FIFOs need to be masked
11[0]	_P3_Latch_OE/src_data	0x00002C	0
11[2]	Bunch_Ctr_FF_Mask	"	0 if the Bunch Counter FIFO does not need to be masked
12[7:0]	Strobes for diagnostics	0x000030	00000000
13[0]	parity	0x000034	0 to output $\sum^{\text{Wedge0}} E_T$ summary first; 1 to output $\sum^{\text{Wedge1}} E_T$ summary first

Table 10: Values of registers to be downloaded to CrateSum prior to the beginning of a run.

4.4 Error Handling/Board Status

The Level 1 data pipeline should not exceed 42 stages. Level 1 accept or reject signals are expected to come every CDF_CLK cycle, starting before the 42nd clock cycle after the first data event. Hence the L1FIFOs are not expected to ever reach their capacity of storage. However, should such situations occur, this is a very serious error and should be signaled immediately.

The Controller stores the status of an error bit, called "board_error". This bit goes high if the full flag of any FIFO on the board is asserted, unless this flag is ignored because its full FIFO masking bit is set. The error bit is placed on CS-P2 and is detected by the TRACER. Diagnostics, including VME instructions to read all FIFO full flags, must be run in order to study any errors and their origins. See Reference [17] for further details.

5 Diagnostics

5.1 Front Panel Lights

CrateSum has 10 front panel lights which indicate whether various operations are occurring on the board. Listed in descending order from the top of the board, these lights are:

1. Power (Green) : Indicates whether the board is receiving power (+5V).

2. Run (Green) : Is lit if the board is in the "run", or data-taking, mode. It reflects the state of the "run" register bit in the Controller.

3. Clock (Yellow) : Reflects the CDF_CLK signal. Since this LED is managed by the Controller chip, it indicates whether the CDF_CLK is reaching the Controller.

4. VME_Select (Green) : Lights up when the board has been selected for a VME transaction, regardless of whether or not that request results in a successful data transfer.

5. L1_Decision (Yellow) : Lights up whenever the Controller issues a strobe to read out L1FIFOs, which should occur whenever a L1 Decision is received.

6. Load (Yellow) : Is lit when the board is in the "load" mode. This light is the logical complement of the "Run" light. At all times when the board is powered, exactly one of the pair of lights "Run" and "Load" should be on.

7. Halt* (Red) : Is the CDF_HALT* signal.

8. Error (Red) : Reflects the state of the "board_error" register bit in the Controller. If this register is set, this means that the full flag for one or more FIFOs is asserted.

9. EPC1 Disabled (Red) : Reflects the state of the switch which toggles the source of the configuration data for the Controller and Processor PLDs on the board. If this light is ON, configuration data is expected to come via the Bit Blaster Download Connector on the Front Panel. If OFF, program loading is performed automatically by a pair of EPROMs upon board power-up.

10. Parity (Yellow) : Indicates whether the 10-bit $\overset{\text{Wedge0}}{\Sigma}\ \mathrm{E_T}$ or $\overset{\text{Wedge1}}{\Sigma}\ \mathrm{E_T}$ summary is sent in the first stage of the two-step data transfer cycle to PreFRED. This light is ON when $\overset{\text{Wedge0}}{\Sigma}\ \mathrm{E_T}$ is sent first, and is OFF in the other case when $\overset{\text{Wedge1}}{\Sigma}\ \mathrm{E_T}$ is sent first.

5.2 Diagnostic Tests Via VME

Non-full-speed tests of CrateSum can be run via VME transactions. These tests are especially useful for verifying that the Processor is forming the DIRAC energy and trigger bit summaries correctly and for ascertaining that each component on the data path through CrateSum is fully functional. It should be noted that VME diagnostics are of limited use in testing run-time, full-speed, timing-sensitive operations. Only a test involving a 132ns-period CDF_CLK signal and data changing at the same speed on P3 allows for run-time conditions to be approximated. The VME diagnostics available to test CrateSum overlap; that is to say, usually two or more tests can be performed which are capable of determining whether some functionality or component of the board is operational. A detailed description of possible VME diagnostic tests that may be run on CrateSum follows. Note that all diagnostics must be run while in the load mode.

5.2.1 Processor Summary Algorithms

Fake $\overset{\text{DIRAC}}{\Sigma}\ \mathrm{E_T}$ and trigger data can be written directly to the Processor from the VME data bus. Energy and trigger bit summary words are formed by the Processor and can be retrieved from the VME data bus. These results can be compared to that expected.

Energy Processing

Consider first the task of testing whether the Processor is forming the correct energy summaries. The following VME write and read transactions should be performed in the order listed:

1. Write a '1' to CrateSum control register word 11, bit 0 ("_P3_Latch_OE/src_data"; located at VME address '0x00002C'). This disables the chips responsible for latching DIRAC data on the P3 backplane and also flags the Processor to expect input data on the VME data bus.

2. Write into the Processor fake energy data representing the P3 output of the four DIRAC boards making up "Wedge 0". This is done by writing to the address '0x200000'. The following correspondence between fake data and DIRAC board is understood: VME_Data(31:0) = ($\overset{\text{DIRAC3}}{\Sigma}\ E_T$, $\overset{\text{DIRAC2}}{\Sigma}\ E_T$, $\overset{\text{DIRAC1}}{\Sigma}\ E_T$, $\overset{\text{DIRAC0}}{\Sigma}\ E_T$). Data from individual DIRACs are placed on the VME_Data bus so that higher order bus bits correspond to more significant data bits.

3. Write fake "Wedge 1" energy data into the Processor by writing to the address '0x200004'. In this case, VME_Data(31:0) = ($\overset{\text{DIRAC7}}{\Sigma}\ E_T$, $\overset{\text{DIRAC6}}{\Sigma}\ E_T$, $\overset{\text{DIRAC5}}{\Sigma}\ E_T$, $\overset{\text{DIRAC4}}{\Sigma}\ E_T$).

4. Retrieve the two 10-bit summaries formed by the Processor by performing a read transaction at address '0x400018'. The bits on the data bus are: VME_Data(31:0) = (unused (12), $\overset{\text{Wedge1}}{\Sigma}\ E_T$ (10), $\overset{\text{Wedge0}}{\Sigma}\ E_T$ (10)). These summaries may then be compared with expected results.

5. The fake data sent to the Processor is also available for retrieval. A read request to CrateSum at address location '0x400000' or '0x400004' prompts the Processor to place the original "Wedge 0" or "Wedge 1" fake DIRAC data on the VME_Data bus. Again, VME_Data(31:0) = ($\overset{\text{DIRAC3}}{\Sigma}\ E_T$, $\overset{\text{DIRAC2}}{\Sigma}\ E_T$, $\overset{\text{DIRAC1}}{\Sigma}\ E_T$, $\overset{\text{DIRAC0}}{\Sigma}\ E_T$) for "Wedge 0" and VME_Data(31:0) = ($\overset{\text{DIRAC7}}{\Sigma}\ E_T$, $\overset{\text{DIRAC6}}{\Sigma}\ E_T$, $\overset{\text{DIRAC5}}{\Sigma}\ E_T$, $\overset{\text{DIRAC4}}{\Sigma}\ E_T$) for "Wedge 1".

Trigger Bit Processing

To test the algorithm forming the trigger bit summaries, a similar series of VME instructions can be issued. These are listed in detail below:

1. Write a '1' to CrateSum control register word 11, bit 0 ("_P3_Latch_OE/src_data"; located at VME address '0x00002C'). This disables the chips responsible for latching DIRAC data on the P3 backplane and also flags the Processor to expect input data on the VME_Data bus.

2. Write into the Processor fake trigger bit data representing the P3 output of the eight DIRAC boards served by CrateSum. This is done by writing to the addresses '0x300000', '0x300004', '0x300008', and '0x30000C', where each address represents data for four trigger bits from each of the eight DIRAC boards (which make up a "Quarter" of the total trigger bit information). For example, "Quarter 1" corresponds to address '0x300000' and the following map between fake data, DIRAC board, and trigger bit is understood: VME_Data(31:0) = (BIT3(DIRAC7) ..... BIT3(DIRAC0), BIT2(DIRAC7) ..... BIT2(DIRAC0), BIT1(DIRAC7) ..... BIT1(DIRAC0), BIT0(DIRAC7) ..... BIT0(DIRAC0)). Likewise, "Quarter 2"/"Quarter 3"/"Quarter 4" correspond to addresses '0x300004'/'0x300008'/'0x30000C' and denote trigger bits (7 to 4)/(11 to 8)/(15 to 12).

3. Retrieve the two 10-bit summaries formed by the Processor by performing a read transaction at address '0x40001C'. The bits on the data bus are: VME_Data(31:0) = (unused (12), TRIG(19:0)), where the meaning of the CrateSum output bit TRIG(x) is given in table 1. These summaries may then be compared with expected results.

4. In addition, the original fake data sent to the Processor is also available for retrieval. A read request to CrateSum at address locations '0x400008', '0x40000C', '0x400010', or '0x400014' prompts the Processor to place the fake trigger bit data from Quarter 1, Quarter 2, Quarter 3, or Quarter 4 on the VME_Data bus. The correspondence between the VME_Data bus bits and the DIRAC board and trigger bits is the same as that given previously for loading fake trigger bit data into the Processor.

5.2.2 FIFOs and Buffers

By extending the set of VME instructions listed above, the L1FIFOs and buffers may be tested. Once fake DIRAC data has been loaded to the Processor via VME, various strobes may be issued to latch the summarized data in the Processor proper and into FIFOs, and to write FIFO data to the appropriate buffers.

Loading the FIFOs

When fake data is written to the Processor via VME, the Processor immediately places this data on the bus lines that ordinarily (i.e. during run-time) bring output data from the P3 latches to the Processor and to the FIFOs responsible for storing raw DIRAC data (ET_Raw and Trig_Raw FIFOs). After the Processor's outputs are stable, the Controller generates strobe signals to latch this data into the appropriate ET_Raw or Trig_Raw FIFOs. Note that is done AUTOMATICALLY, in the same cycle as that in which the fake data is loaded into the Processor. There is no need, during this particular diagnostic test, to manually issue the "L1FIFO_Wclk_ET_Raw" or "L1FIFO_Wclk_Trig_Raw" strobes (CrateSum control register word 12, bits 6 and 7; VME Address '0x000030'). The purposes of these strobes will be made clear later when other diagnostic avenues are discussed.

Loading the ET_Sum and Trig_Sum FIFOs requires that the Processor latches its own summaries first. Then the summary words can be written into the appropriate FIFOs.

Assuming that fake data have already been loaded into the Processor in the manner described in the previous sections, the additional steps to be taken are as follows:

1. Issue strobes to latch the $\overset{\text{Wedge}}{\Sigma}$ E_T and trigger bit summaries inside the Processor by writing a '1' to the CrateSum control registers "proc_latch_clk_ET" and "proc_latch_clk_Trig", respectively (word 12, bits 0 and 2; VME address '0x000030'). This step could be performed as part of the summary algorithm diagnostic procedures listed above, although it is not required for that test.

2. Load the $\overset{\text{Wedge}}{\Sigma}$ E_T and trigger bit summaries into the ET_Sum and Trig_Sum FIFOs by writing a '1' to the registers "L1FIFO_Wclk_ET_Sum" and "L1FIFO_Wclk_Trig_Sum", respectively (word 12, bits 1 and 3; VME address '0x000030').

The Bunch Counter L1FIFO can be tested by first writing a fake number to the Controller. This is done by issuing a write transaction to the VME address '0x500000' and placing the 8-bit value on the upper 8 bits of the VME_Data bus. This prompts the Controller to send these bits to the input of the Bunch Counter and to issue a strobe to latch this number into the FIFO.

There is no way to look at the outputs of the FIFOs directly. First the data must be sent to sent to buffers. From there, the data can be read out via VME transfers.

Loading and Reading the Buffers

After the L1FIFOs have been loaded with fake data, they may be sent to the L2 buffers. There is no need to unload the first set of data from the FIFOs, as it is immediately available at the outputs. The following steps should be followed:

1. Pick one of the four buffer locations (binary '00', '01', '10', or '11'). Then prompt the Controller to issue a load command to this particular buffer location by writing to the "L2B_W" and "L2B[1:0]" registers in the Controller (word 3, bits 3, 5, and 6; VME address '0x00000C').

2. If there are other events in the FIFO, unload the next set of data onto the output lines of the FIFOs by issuing a "FIFO_Rclk" command (word 3, bit 2; VME address '0x00000C'). Even if there are no additional events in the FIFOs, such a command may be issued and will merely result in the placement of null values at the outputs without any adverse effects.[13] Hence it may be advisable to always issue a "FIFO_Rclk" command following a FIFO write cycle to a buffer location, as this will ensure that the next set of data is immediately available for sending to another buffer location, without having to recall whether this data has been previously unloaded or not.

3. After the fake raw and summed data is written into the buffers, it may then be read out. This is done by issuing exactly the same set of commands as in a datastream readout in the trigger diagnostic mode. The VME address locations to read from are

[13] In fact, the next set of data will then be available at the outputs as soon as it is written in to the FIFOs.

listed in Table 9. These results can be examined to make sure no corruption of the raw or summed data has occurred in its passage through the L1FIFOs and the L2 buffers.

4. The above steps may be repeated for each of the other buffer locations.

5.2.3 Testing the P3 Latches

These latches cannot be tested entirely through VME transactions, since they latch only data from P3 and not data from the VME_Data bus. However, if test raw DIRAC data is made available on the J3 backplane/P3 connector, most of the steps involved in testing the P3 latches can be performed using VME transfers in the manner described below:

1. Make sure that the "_P3_Latch_OE/src_data" register is set to '0'. This enables the P3 latches and tells the processor to expect data to come from P3.

2. Latch the raw $\overset{\text{DIRAC}}{\Sigma}$ E_T and trigger bit data from P3 by writing a '1' to the "P3_Latch_clk_ET" and "P3_Latch_clk_Trig" registers, respectively, in the Controller (word 12, bits 4 and 5; VME address '0x000030').

3. Now the $\overset{\text{Wedge}}{\Sigma}$ E_T and trigger bit summaries, as well as the original data at the P3 connector, can be read out by reading from VME address locations '0x400000' through '0x40001C', as described in the section above concerning Processor summary algorithm testing.

4. Alternatively, the test data placed on P3 can also find its way through the board by way of the L1FIFOs and L2 buffers. This is done by issuing FIFO load strobes and buffer write commands in exactly the same manner as that described above for testing the functionality of the FIFOs and buffers. However, in this case of test data from P3, one must explicitly send VME commands to the Controller prompting it to issue strobes for loading ET_Raw and Trig_Raw L1FIFOs. Since all raw $\overset{\text{DIRAC}}{\Sigma}$ E_T and trigger bit test data are available at the same time at the outputs of the P3 latches, load instructions can be issued at the same time for the different energy "wedges" or trigger bit "quarters".[14] By writing a '1' to the "L1FIFO_Wclk_ET_Raw" or "L1FIFO_Wclk_Trig_Raw" registers (Control register word 12, bits 6 and 7; VME address '0x000030'), the Controller issues load commands at the same time to the various ET_Raw or Trig_Raw FIFOs. The summary data can be latched inside the Processor and sent to the ET_Sum and Trig_Sum L1FIFOs by issuing the same VME commands as those described in the section above about testing the FIFOs. After loading all data in the FIFOs, they can then be stored in the L2 buffers and read out. The procedure for doing this has also been discussed previously.

[14] This is not the case for writing test data to the processor via the VME_Data bus, in which case the L1FIFO write strobes are generated automatically by the Controller. In that situation, the fact that the bus is 32 bits wide limits raw test data to be loaded in the appropriate ET_Raw or Trig_Raw FIFOs in individual "wedges" or "quarters" sequentially. Thus the different FIFOs are controlled by independent write signals.

5.2.4 Testing the DIRAC Board Masking Bits

During actual data-taking, certain parts of the detector may be dysfunctional and it may be required that their data at downstream locations be masked. CrateSum allows for the inputs from one or more DIRAC boards to be ignored. If a board is masked, the data coming from it becomes transparent to the Processor. The Processor will regard the data coming from this DIRAC board as consisting of null values. To verify that this masking feature works, follow these steps:

1. First write to the "Mask_DIRAC[7:0]" registers (word 4; VME address '0x000010'). The bits in this word should be set to '1' according to which DIRAC boards are to be masked. The eight DIRAC boards serviced by CrateSum are labeled from 0 to 7 in order of increasing slot number.

2. Now run any or all of the diagnostic tests described above to verify that masking of the targeted DIRAC board(s) has occurred.

5.2.5 FIFO Full and Empty Flags

The state of the ET_Raw, Trig_Raw, ET_Sum, and Trig_Sum FIFO full and empty flags may be determined by reading from words 7, 8, 9, and 10 of CrateSum's control registers. These correspond to VME addresses '0x00001C', '0x000020', '0x000024', and '0x000028'. To find out the values of the Bunch Counter FIFO full and empty flags, read from the "FF_Bunch_Ctr" and "EF_Bunch_Ctr" registers (word 13, bits 2 and 3; VME address '0x000034'). See Table 6.

The "board_error" bit in the Controller is asserted if any FIFO full flag is set. If it is desired that the full flag of any ET or trigger bit FIFO be masked (i.e. made transparent to the logic that determines the value of the "board_error" bit), the appropriate register in words 5 and 6 can be set (VME addresses '0x000014' and '0x000018'). To mask the Bunch Counter FIFO full flag, write a '1' to word 11, bit 2. Again, please refer to Table 6.

The FIFO full flags and the board error bit can be tested by filling up one or more FIFOs. Writing these events to the FIFOs can be done in either of the two ways described previously, through VME transactions or directly through the J3 backplane/P3 connector. After 256 events have been stored in the FIFOs, the full flag should be asserted and the board error bit set. The "board_error" bit is located at word 13, bit 1 (VME address '0x000034').

The FIFO full flag masking bits can be tested by masking one or more FIFOs and filling the masked FIFOs up by writing 256 events. In this case, the board error bit should not be set.

At any time (in load mode), the FIFOs and the board error bit may be reset by setting the "recover" register to '1' (word 3, bit 1; VME address '0x00000C').

5.2.6 Version Numbers

To determine the current versions of the Controller or Processor programs, read from words 14 and 15 (VME addresses '0x000038' and '0x00003C'). At this time, version numbers of the programs are set to '1' and are not incremented when changes are made. Version numbers will not change until data-taking begins in earnest and it becomes necessary to document the programs in effect at the time when data is processed.

5.2.7 Module ID PROM Word

The ID PROM is a string of 32 ASCII characters used to identify an individual module or map the location of all such modules in a crate. CrateSum stores these 32 eight-bit words at VME addresses '0x100000' to '0x10007C'. In order of increasing address number, the contents of these addresses are:

1. 2 characters: '00'.
2. 2 characters: Board serial number, a value between 1 and 20, written in base 10.
3. 1 character: ASCII blank.
4. 3 characters: Board Type: '010'.
5. 1 character: ASCII blank.
6. 8 characters: 'CRATESUM', written in capital letters.
7. 15 characters: ASCII null.

See Reference [5] for details.

5.2.8 Other Diagnostics

Only a few of the VME diagnostic avenues available for testing CrateSum have been explicitly described above. The meaning of each of the control registers, along with the contents of CrateSum's VME address locations, have been discussed in detail. This permits the astute physicist to come up with various original and imaginative testing algorithms which may under certain circumstances be more appropriate for testing specific parts of the board than the standard tests described in this document.

5.3 Probing Board Signals

In addition to the high-level diagnostic tests which may be run through VME transactions, signals on the board itself may be probed. A description of the signal-spying features built into the design belongs more naturally in the board-level design document, so please refer to [3] for this discussion.

Signal Name	Description	Used by CS?
CLK	Differential PECL Clock signal (132ns)	**Yes**
CLK*	Differential PECL Clock signal (132ns)	**Yes**
BC*	Bunch Crossing	No
B0*	Bunch 0	**Yes**
L1A*	Global Level 1 Accept Signal	**Yes**
L1R*	Global Level 1 Reject Signal	**Yes**
L2B0*	Level 1 Accept Buffer Address 0	**Yes**
L2B1*	Level 1 Accept Buffer Address 1	**Yes**
HALT*	Stop filling L1 FIFO/pipelines and processing events.	**Yes**
RECOVER*	Master Reset; Reset FIFOs and Pipelines	**Yes**
ABORT*	Dump Everything	No
CALIB0*	Calibration bit 0	No
⋮	⋮	⋮
CALIB6*	Calibration bit 6	No
CALEN*	Calibration Enable	No
ERROR*	Error bit sent to TSI in the event of an error in the L1 Crate.	**Yes**
L2A*	Global Level 2 Accept Signal	No
L2R*	Global Level 2 Reject Signal	No
L2A_EN*	L2 Accept Enable Signal	No
L2BD0*	L2 Accept Decision Buffer Address Bit 0	No
L2BD1*	L2 Accept Decision Buffer Address Bit 1	No
RSVD0*	Reserved bit	No
RSVD1*	Reserved bit	No
TDC_CAL0*	TDC Calibration Pulses produced by the TRACER.	No
TDC_CAL1*	TDC Calibration Pulses produced by the TRACER.	No
TDC_CAL2*	TDC Calibration Pulses produced by the TRACER.	No
TDC_CALIB	Precision TDC Calibration Pulse	No
TDC_CALIB*	Precision TDC Calibration Pulse	No
TDC_DONE*	Indicates that TDCs have moved data into local L2 buffers.	No
GLIVE*	L1 Accept corresponds to live Beam Crossing	No
RSVD_L1W1*	TSI reserved L1 word bit(7)	No
RSVD_L1W2*	TSI reserved L1 word bit(8)	No
STOP*	Set Halt Condition	No
TEST*	Diagnostic Bit	No
RUN*	Clear Halt Condition	No
RL0*	Readout List Identifier bit	No
RL1*	Readout List Identifier bit	No
RL2*	Readout List Identifier bit	No
EVID0*	Event Identifier bit 0	No
EVID1*	Event Identifier bit 1	No
EVID2*	Event Identifier bit 2	No
EVID3*	Event Identifier bit 3	No

Table 11: Signals sent from the Trigger System Interface along CS-P2. Signal names are preceeded by the prefix "CDF_". All signals are TTL levels and active low, with the exception of CLK, CLK*, TDC_CALIB, and TDC_CALIB* (differential PECL) and ERROR and TDC_DONE (open collector). Details can be found in CDF Note 2388 (July 1997).

PIN	Row					Comments
	z	A	B	C	d	
1	V	Term Usr Bus		TDC_CAL0*	V	
2	M	Term Usr Bus		TDC_CAL1*	M	
3	E	Term Usr Bus		TDC_CAL2*	E	
4	6	Term Usr Bus		TDC_CALIB	6	(CMOS)
5	4	Term Usr Bus	S	TCD_CALIB*	4	
6		CLK	T	TDC_DONE		132ns (7 RF Bucket) Clock
7	E	CLK*	A	Term Usr Bus	E	DIFF (PECL)
8	x	Term Usr Bus	N	Term Usr Bus	x	
9	t	BC*	D	Term Usr Bus	t	Beam Crossing Indicator (TTL Active Low)
10	e	B0*	A	Term Usr Bus	e	Bunch 0 Indicator (TTL Active Low)
11	n	Term Usr Bus	R	Term Usr Bus	n	
12	s	L1A*	D	GLIVE*	s	L1 Accept (TTL Active Low)
13	i	L1R*		L1W1*	i	L1 Reject (TTL Active Low)
14	o	L2B0*		L2W2*	o	L1A buffer address 0 (TTL Active Low)
15	n	L2B1*		STOP*	n	L1A buffer address 1 (TTL Active Low)
16	s	HALT*		TEST*	s	Halt Filling L1 Pipeline
17		Term Usr Bus	V	RUN*		
18	S	RECOVER*	M	RL0*	S	Reset FIFOs/Buffers (TTL Active Low)
19	t	Term Usr Bus	E	RL1*	t	
20	a	ABORT*	b	RL2*	a	Abort Gap starting (TTL Active Low)
21	n	CALIB0*	u	CALIB3*	n	Calibration enable 0 (TTL Active Low)
22	d	Term Usr Bus	s	CALIB4*	d	
23	a	CALIB1*		CALIB5*	a	Calibration enable 1 (TTL Active Low)
24	r	CALIB2*		CALIB6*	r	Calibration enable 2 (TTL Active Low)
25	d	Term Usr Bus		CALEN*	d	
26		ERROR*		Term Usr Bus		Error on card (Output OC TTL)
27	P	L2A*		L2R*	P	L2 Accept (TTL Active Low)
28	i	L2BD0*		L2A_EN*	i	L2A Buffer Address 0 (TTL Active Low)
29	n	Term Usr Bus		EVID0*	n	
30	o	L2BD1*		EVID1*	o	L2A Buffer Address 1 (TTL Active Low)
31	u	RSVD0*		EVID2*	u	
32	t	RSVD1*		EVID3*	t	

Table 12: Pin assignments for the Standard VME CS-P2 connector to the J2 Backplane. Rows z and d follow the VME64 Extensions Standard Pinout specification. The middle row, Row B, is dedicated for standard VMEbus signals. Rows A and C are used to distribute timing signals from the TRACER. All “Term Usr Bus” lines in rows A and C are reserved. They are terminated in the same way that VMEbus address/data lines are.

Signals sent from DIRAC

Signal Name	Description
ETSUM(7)	E_T Most Significant Bit
ETSUM(6)	E_T Next-to-Most Significant Bit
$\vdots$	$\vdots$
ETSUM(1)	E_T Next-to-Least Significant Bit
ETSUM(0)	E_T Least Significant Bit
TRSUM(15)	Trigger bit 15
TRSUM(14)	Trigger bit 14
TRSUM(13)	Trigger bit 13
TRSUM(12)	Trigger bit 12
$\vdots$	$\vdots$
TRSUM(3)	Trigger bit 3
TRSUM(2)	Trigger bit 2
TRSUM(1)	Trigger bit 1
TRSUM(0)	Trigger bit 0

Table 13: Signals passed from DIRAC to CrateSum along the J3 backplane.

Pin #	z	a	b	c	d	e	f
1	GND	TRSUM0(2)	TRSUM0(1)	TRSUM0(0)	TRSUM7(1)	TRSUM7(0)	GND
2	GND	TRSUM0(4)	TRSUM0(3)	GND	TRSUM7(3)	TRSUM7(2)	GND
3	GND	TRSUM0(7)	TRSUM0(6)	TRSUM0(5)	TRSUM7(5)	TRSUM7(4)	GND
4	GND	TRSUM0(9)	TRSUM0(8)	GND	TRSUM7(7)	TRSUM7(6)	GND
5	GND	TRSUM0(11)	TRSUM0(10)	TRSUM7(10)	TRSUM7(9)	TRSUM7(8)	GND
6	GND	TRSUM0(13)	TRSUM0(12)	GND	TRSUM7(12)	TRSUM7(11)	GND
7	GND	TRSUM0(15)	TRSUM0(14)	TRSUM7(15)	TRSUM7(14)	TRSUM7(13)	GND
8	GND	TRSUM1(2)	TRSUM1(1)	TRSUM1(0)	TRSUM6(1)	TRSUM6(0)	GND
9	GND	TRSUM1(4)	TRSUM1(3)	GND	TRSUM6(3)	TRSUM6(2)	GND
10	GND	TRSUM1(7)	TRSUM1(6)	TRSUM1(5)	TRSUM6(5)	TRSUM6(4)	GND
11	GND	TRSUM1(9)	TRSUM1(8)	GND	TRSUM6(7)	TRSUM6(6)	GND
12	GND	TRSUM1(11)	TRSUM1(10)	TRSUM6(10)	TRSUM6(9)	TRSUM6(8)	GND
13	GND	TRSUM1(13)	TRSUM1(12)	GND	TRSUM6(12)	TRSUM6(11)	GND
14	GND	TRSUM1(15)	TRSUM1(14)	TRSUM6(15)	TRSUM6(14)	TRSUM6(13)	GND
15	GND	TRSUM2(2)	TRSUM2(1)	TRSUM2(0)	TRSUM5(1)	TRSUM5(0)	GND
16	GND	TRSUM2(4)	TRSUM2(3)	GND	TRSUM5(3)	TRSUM5(2)	GND
17	GND	TRSUM2(7)	TRSUM2(6)	TRSUM2(5)	TRSUM5(5)	TRSUM5(4)	GND
18	GND	TRSUM2(9)	TRSUM2(8)	GND	TRSUM5(7)	TRSUM5(6)	GND
19	GND	TRSUM2(11)	TRSUM2(10)	TRSUM5(10)	TRSUM5(9)	TRSUM5(8)	GND
20	GND	TRSUM2(13)	TRSUM2(12)	GND	TRSUM5(12)	TRSUM5(11)	GND
21	GND	TRSUM2(15)	TRSUM2(14)	TRSUM5(15)	TRSUM5(14)	TRSUM5(13)	GND
22	GND	TRSUM3(2)	TRSUM3(1)	TRSUM3(0)	TRSUM4(1)	TRSUM4(0)	GND
23	GND	TRSUM3(4)	TRSUM3(3)	GND	TRSUM4(3)	TRSUM4(2)	GND
24	GND	TRSUM3(7)	TRSUM3(6)	TRSUM3(5)	TRSUM4(5)	TRSUM4(4)	GND
25	GND	TRSUM3(9)	TRSUM3(8)	GND	TRSUM4(7)	TRSUM4(6)	GND
26	GND	TRSUM3(11)	TRSUM3(10)	TRSUM4(10)	TRSUM4(9)	TRSUM4(8)	GND
27	GND	TRSUM3(13)	TRSUM3(12)	GND	TRSUM4(12)	TRSUM4(11)	GND
28	GND	TRSUM3(15)	TRSUM3(14)	TRSUM4(15)	TRSUM4(14)	TRSUM4(13)	GND
29	GND	GND	GND	GND	GND	GND	GND
30	GND	ETSUM3(1)	ETSUM3(0)	GND	ETSUM4(1)	ETSUM4(0)	GND
31	GND	ETSUM3(3)	ETSUM3(2)	GND	ETSUM4(3)	ETSUM4(2)	GND
32	GND	ETSUM3(5)	ETSUM3(4)	ETSUM4(6)	ETSUM4(5)	ETSUM4(4)	GND
33	GND	ETSUM3(7)	ETSUM3(6)	GND	ETSUM5(0)	ETSUM4(7)	GND
Connector Key (equivalent to 3 pins)							
34	GND	ETSUM2(1)	ETSUM2(0)	GND	ETSUM5(2)	ETSUM5(1)	GND
35	GND	ETSUM2(3)	ETSUM2(2)	GND	ETSUM5(4)	ETSUM5(3)	GND
36	GND	ETSUM2(6)	ETSUM2(5)	ETSUM2(4)	ETSUM5(6)	ETSUM5(5)	GND
37	GND	ETSUM1(0)	ETSUM2(7)	GND	ETSUM6(0)	ETSUM5(7)	GND
38	GND	ETSUM1(2)	ETSUM1(1)	GND	ETSUM6(2)	ETSUM6(1)	GND
39	GND	ETSUM1(4)	ETSUM1(3)	GND	ETSUM6(4)	ETSUM6(3)	GND
40	GND	ETSUM1(6)	ETSUM1(5)	ETSUM6(7)	ETSUM6(6)	ETSUM6(5)	GND
41	GND	ETSUM0(0)	ETSUM1(7)	GND	ETSUM7(1)	ETSUM7(0)	GND
42	GND	ETSUM0(2)	ETSUM0(1)	GND	ETSUM7(3)	ETSUM7(2)	GND
43	GND	ETSUM0(4)	ETSUM0(3)	GND	ETSUM7(5)	ETSUM7(4)	GND
44	GND	ETSUM0(7)	ETSUM0(6)	ETSUM0(5)	ETSUM7(7)	ETSUM7(6)	GND

Table 14: Pin assignments for the CrateSum P3 connector on the J3 Backplane. The number at the end of the signal name is the DIRAC within the half-crate from which the signal came. (See Figure 2.) The number in parentheses is the bit number with 0 as the least significant bit. For example, ETSUM2(6) is the E_T next-to-most significant bit from DIRAC board 2.

References

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[17] A. Amadon *et al.*, *Error Detection and Handling for the Calorimeter Trigger*, Trigger Note #98, Jan. 1998.

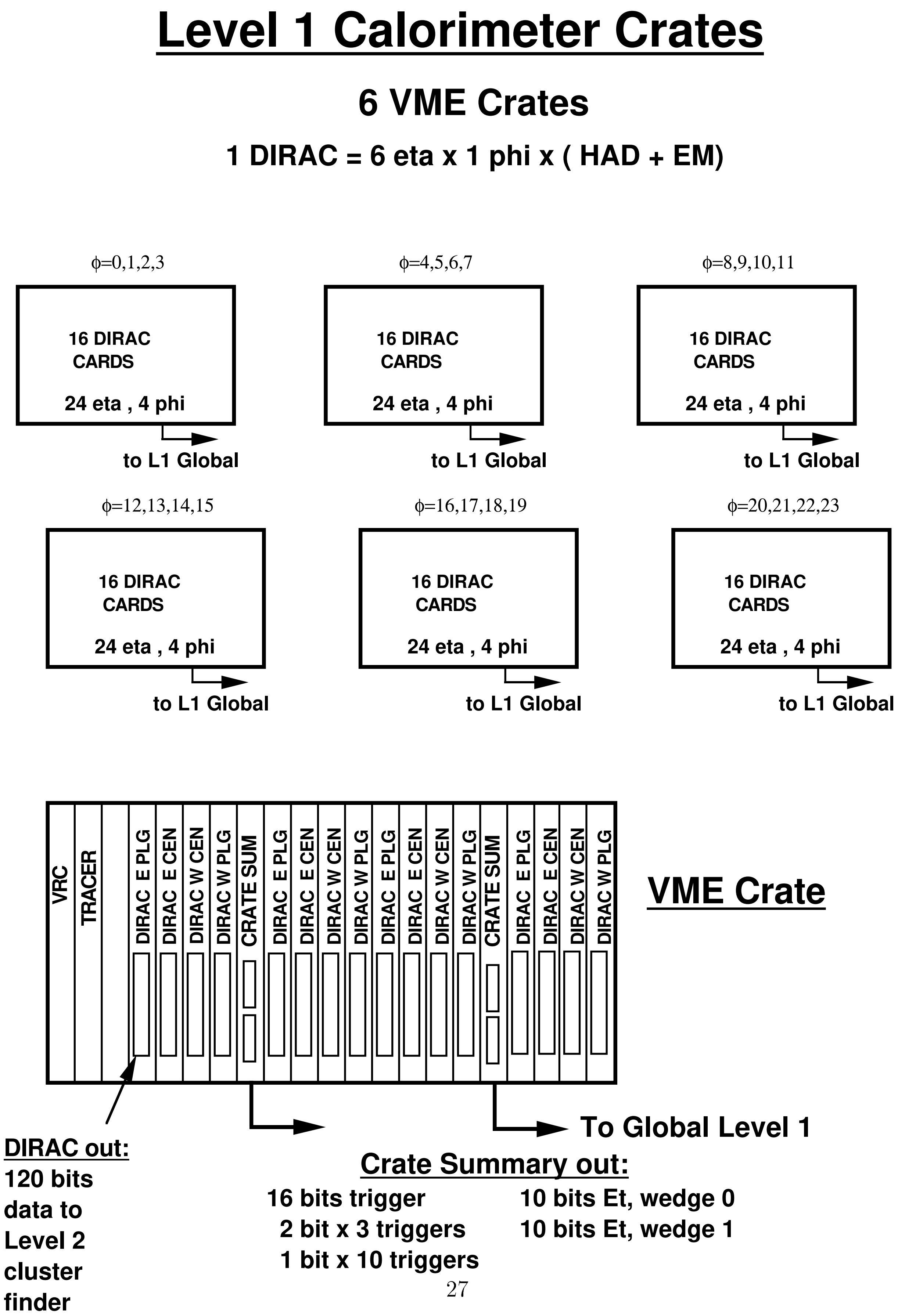

Figure 1: Physical Structure of the L1 Crate Layout.

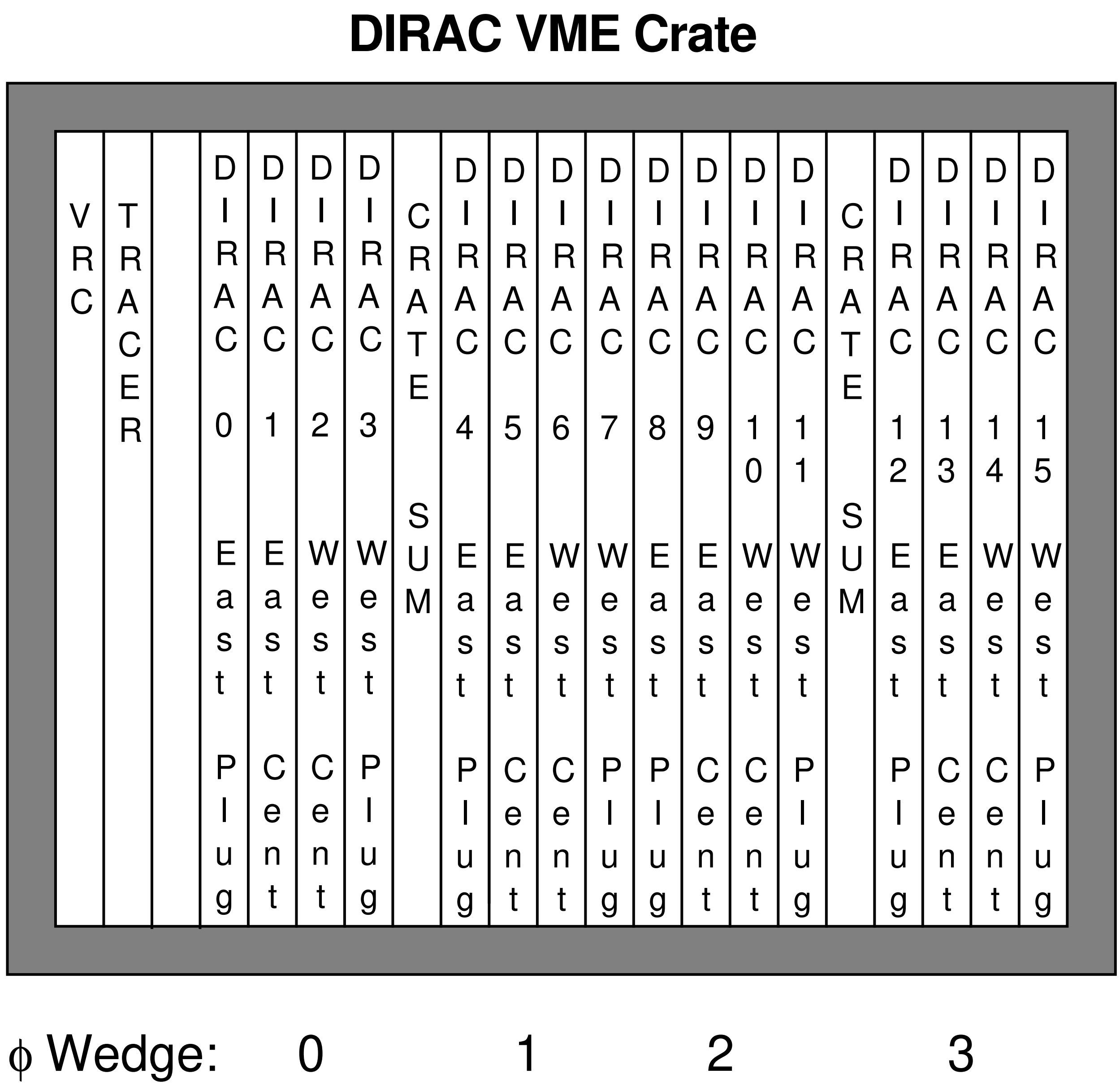

Figure 2: Physical Structure of the Crate. Note that this setup reflects the fact that the upgrade CAS equivalent will not lie in this crate as it is no longer used in a L1 decision. Also note that the CrateSum card is in the center of the eight DIRAC boards from which it accepts signals. There are 21 slots in the crate, labeled starting from 1. The two CrateSum boards are located at slots 8 and 17.

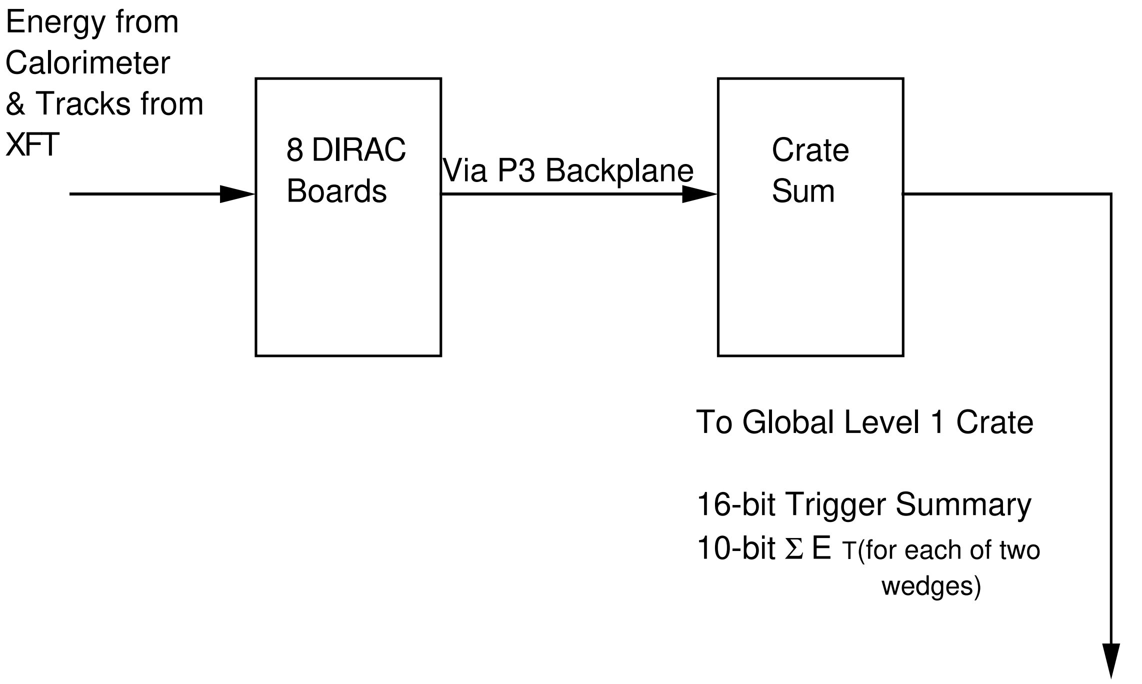

Figure 3: Level 1 Data Flow.

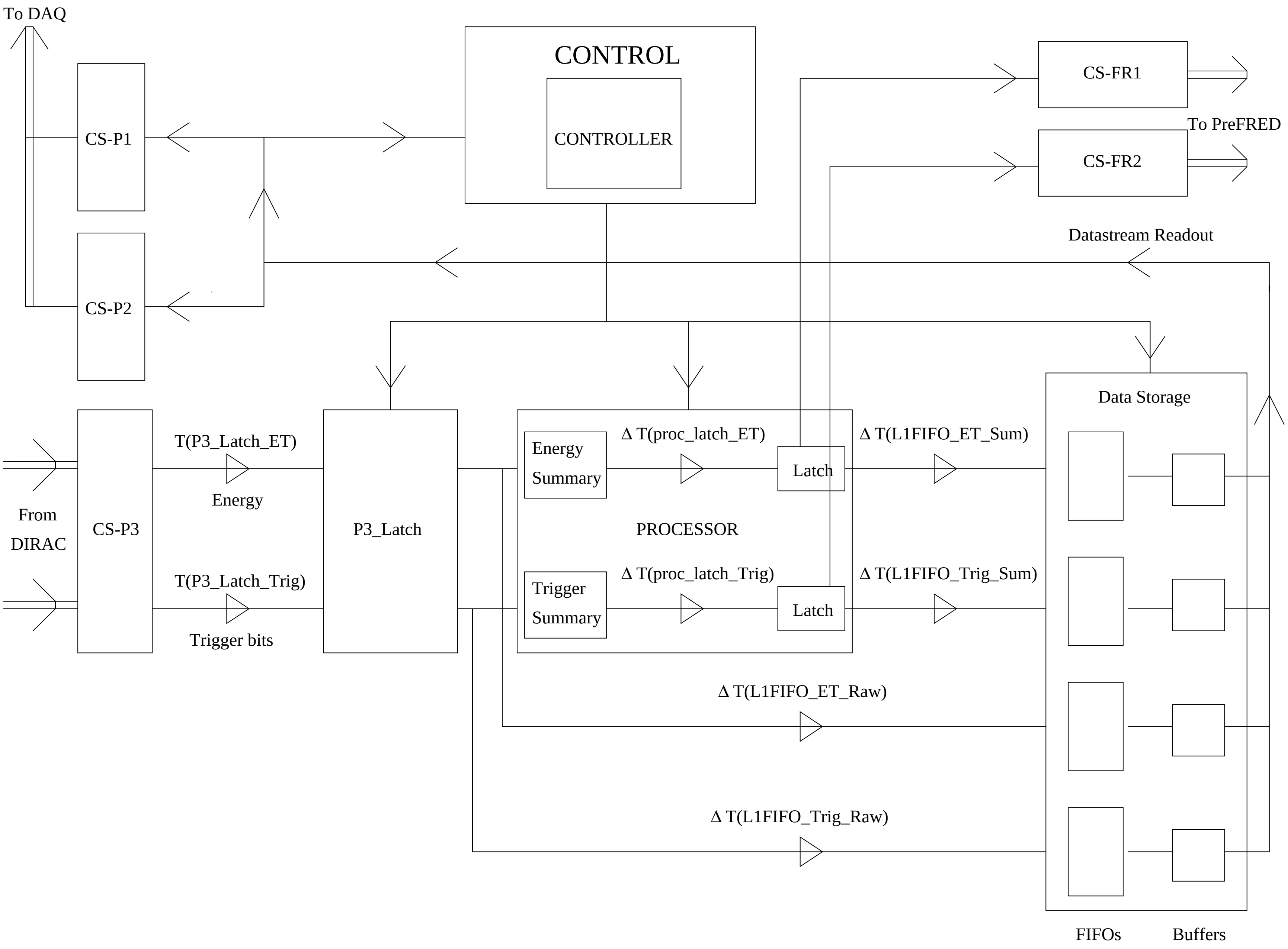

Figure 4: CrateSum Functional Schematic

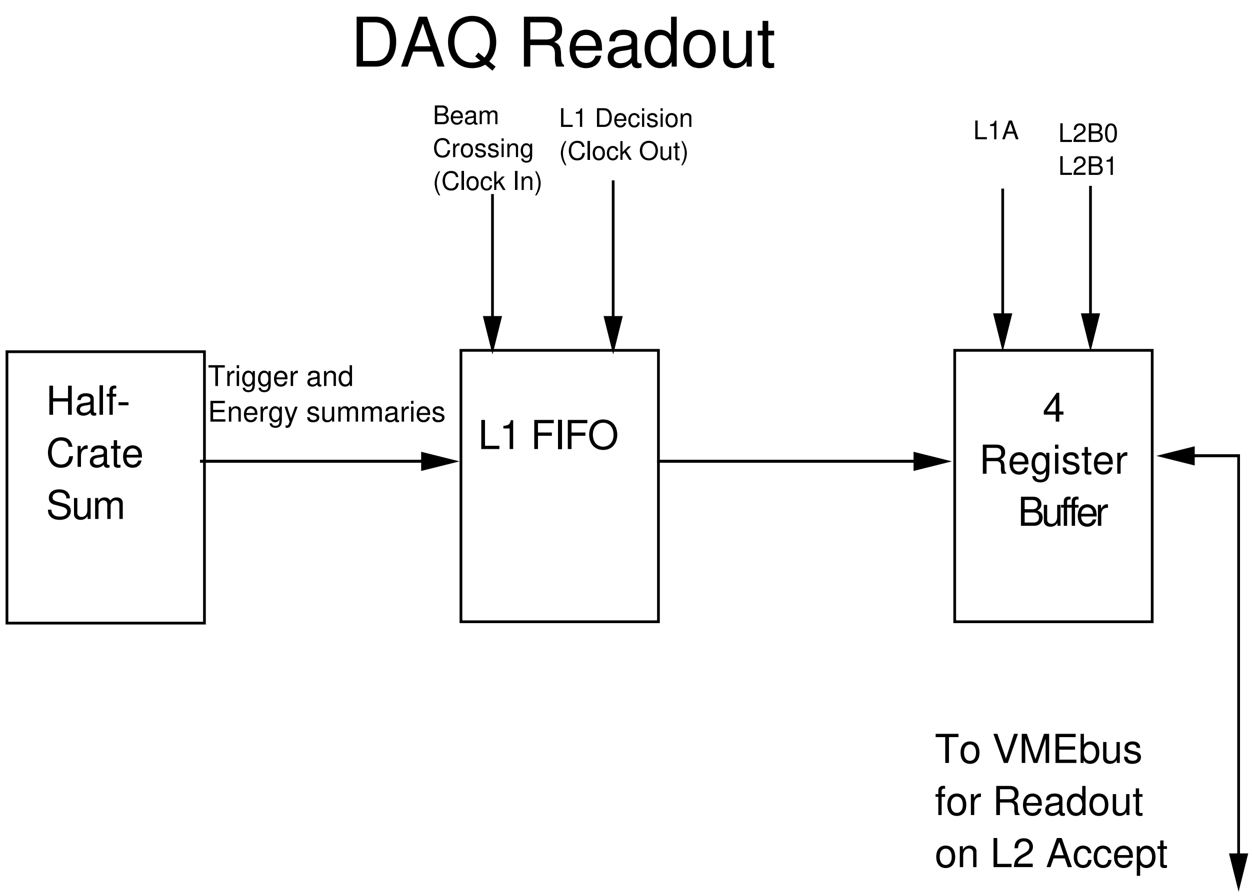

Figure 5: Event Readout Diagram