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CrateSum
Upgrade for Run II

1 Introduction and Overview

The upgraded Level 1 calorimetry trigger planned for Run II will be entirely digital, deadtimeless and designed to accommodate shorter bunch spacings, higher trigger bandwidth and the plug upgrade [1, 2]. This note describes the purpose and functionality of the new CrateSum (CS) board within the context of this new system. Detailed information on the design and hardware implementation of this board can be found in Reference [3].

The role of each calorimetry trigger crate will be the same as in Run I [4], except that it will only be used in Level 1 (L1). See Figures 1 and 2 for a schematic of the system and the crate layout. Each crate will calculate $\overset{\text{Wedge}}{\Sigma}\,\mathrm{E_T}$ for each of four wedges. ($\overset{\text{Wedge}}{\Sigma}\,\mathrm{E_T}$ is the transverse energy summed over all η for both Hadronic (Had) and Electromagnetic (EM) calorimeters in one 15 degree wedge in the azimuthal angle ϕ.) Each crate will also use tracking to help determine how many trigger towers pass various triggers. The standard CDF upgrade crate setup [5] includes two CrateSum[1] boards and sixteen Digital Information Receive and Compare (DIRAC) boards [6] within each crate. Each DIRAC uses calorimetry tower energy and tracking information to decide which towers pass a given trigger. DIRAC also sums up the total energy deposited in its towers above a given threshold. Both results are passed to a CrateSum board along a custom backplane. CrateSum uses information from eight (consisting of two sets of four) DIRACs to summarize the triggers passed and to compute the total energy deposited in each of the two groups of four boards. These results are carried by front panel connectors to a PreFRED module [7] for further processing and are ultimately sent to the Global Level 1 crate for a L1 decision.

2 Level 1 Calorimetry Crate Functional Description

2.1 The Standard CDF VME Crate and Backplanes

The standard CDF upgrade crate is a 9U VME crate and contains a Motorola MVME2301 VMEbus Readout Controller (VRC) and a **TR**igger **A**nd **C**lock + **E**vent **R**eadout (TRACER) Module [8] to interface with the DAQ system and the Trigger System Interface (TSI)[2]

[1]In the upgrade, it's really a "Half-Crate" Sum.

[2]The VRC, TSI, and the TRACER will be referred to as the DAQ when VME interactions are under discussion. Although the VRC and the TRACER modules pass on control signals from the TSI to CrateSum, such communications initiated or received by the TSI will simply be referred to as being made with the TSI without mention of the VRC and TRACER.

There are two backplanes in the readout crate. The upper backplane is a CDF standard backplane and has three connectors for each slot. These are P1, P0, and P2, listing them in order from the top to bottom. (The associated backplane segments are called J1, J0, and J2, respectively.) P1 is the standard 5-row VME-P P1 [10] connector with 32 pins in each row. P0 is a power connection that is not used by CrateSum. P2 is a connector with five rows of pins. The middle row of pins on P2 are for standard VME signals and the two rows on either side are reserved for global CDF control signals. For CrateSum, these rows are used to pass the TSI control signals from the TRACER module. The outermost two rows are defined in the VME64 Extensions Draft Standard [11].

The second backplane, J3, has been custom-built to pass point-to-point signals between DIRAC and CrateSum and is described in detail in [12]. The boards are placed as shown in Figure 2. Note that each CrateSum receives signals from eight DIRACs, four on each side. Each set of four DIRACs on each side of CrateSum receives signals from an entire ϕ wedge ($-3.51 \leq \eta \leq 3.51$ for both Had and EM).

2.2 DIRAC

The overall data flow chart for the L1 calorimetry crate is shown in Figure 3. Since the $\eta - \phi$ map for both the physical and trigger towers has changed from that used in Run 1 [13], each DIRAC will now take in 12 trigger towers with the same ϕ, half from the Had calorimeter and half from the EM. For each tower, DIRAC reads in 10 bits of $\mathrm{E_T}$ data from the Front-End with 0.125 GeV least count and 128 GeV full scale[3]. This information is used in conjunction with the tracking information from the XFT to determine how many towers, if any, on the board satisfy each of a number of triggers. The results are stored as a 16-bit word which consists of ten 1-bit trigger results (pass/nopass) and three 2-bit trigger results (0, 1, 2 or ≥ 2 trigger towers passing). In addition, DIRAC forms an 8-bit $\overset{\mathrm{DIRAC}}{\Sigma}\ \mathrm{E_T}$ word with 0.5 GeV least count and 128 GeV full scale for all towers above some shoulder $\mathrm{E_T}$ value. These two summaries from one DIRAC card are placed on the J3 backplane along with the results from seven other DIRAC cards and passed to the appropriate CrateSum board. Note that the energy summing on DIRAC occurs before the tracking information arrives, and can be passed on to CrateSum before the trigger summary is completed. Thus, the energy summing and trigger summary sections work independently. For a more complete description of DIRAC, see Reference [6].

2.3 CrateSum

Since the $\overset{\mathrm{DIRAC}}{\Sigma}\ \mathrm{E_T}$ and trigger words from the DIRAC cards may be available at different times, CrateSum begins the process of making an energy or trigger summary by latching either the eight trigger words or eight $\overset{\mathrm{DIRAC}}{\Sigma}\ \mathrm{E_T}$ words on the J3 backplane. Since CrateSum receives the $\mathrm{E_T}$ information for all calorimeter towers from two different ϕ wedges (four

[3]Note that the scale is the same as that used in run 1A [14] and is imposed in order to both keep the number of output bits per board to a minimum as well as to keep a large full scale. Note also that placing limitations on the full scale range and energy resolution of the L1 trigger may have consequences for future physics uses.

DIRACs per wedge and two sets of four DIRACs), it produces $\overset{\text{Wedge}}{\Sigma} E_T$ for each wedge. Each of these two 10-bit summaries indicates an E_T between 0 and 512 GeV with 0.5 GeV least count. If the 8-bit word from any DIRAC has all bits set, all bits are turned on in the 10-bit CrateSum E_T summary for that wedge.

On the trigger front, CrateSum has the capability to use the eight 16-bit DIRAC trigger words it receives to produce a maximum 20-bit half-crate summary consisting of any combination of 1-bit, 2-bit, or 3-bit words adding up to a total of 20 bits. The trigger summary program currently provides for eight select lines, controlled externally by the Controller chip, which indicate the type of summing for DIRAC bits 0 and 1, 2 and 3, ... , 14 and 15: either two 8-to-1-bit summaries or one 8-by-2-to-2-bit summary. The 2-bit summaries for the DIRAC bits are labeled as listed in Table 1, and are sent out of the front panel in the order specified in Table 8.

Placement of CrateSum Output Trigger Bits

Trigger Bits	Are formed from DIRAC bits:
Trig(19:18)	(15:14)
Trig(17:16)	(13:12)
Trig(15)	Spare bit
Trig(14:13)	(11:10)
Trig(12:11)	(9:8)
Trig(10)	Spare bit
Trig(9:8)	(7:6)
Trig(7:6)	(5:4)
Trig(5)	Spare bit
Trig(4:3)	(3:2)
Trig(2:1)	(1:0)
Trig(0)	Spare bit

Table 1: Labels for the CrateSum trigger bit summaries. If necessary, the spare bits may be regrouped and placed in one block.

The use of programmable logic devices (PLDs) permits flexiblility in specifying the summary algorithms. Both the E_T and trigger processing programs are implemented in single large PLDs. This allows the trigger summary algorithm, in particular, to be changed should such a change be necessary.

The E_T and trigger summaries are latched into FIFOs and are also sent to the PreFRED modules to be processed for use in the Global Level 1 crate in making a L1 decision. Also stored in FIFOs are the bunch number of the event and the original eight $\overset{\text{DIRAC}}{\Sigma} E_T$ words and eight DIRAC trigger summaries. Storage of both DIRAC and CrateSum energy and trigger summaries on CrateSum is controlled by TSI signals on the J2 backplane. These summaries are read out by the DAQ in the event of a Level 2 accept (L2A).

2.4 Crate Level Datastream Readout

On a L2A, CrateSum may read out the energy and trigger summaries from itself and DIRAC into the datastream. Before this can occur, it must interact with the DAQ as well as with the TSI. The latter gives detailed filtering instructions as to which events need to be stored, which buffers on the board the data are to be stored in, and when they are to be read out. Referring to Figure 5, each board processes its data and stores the result in a pipeline (FIFO) until it receives a L1 decision from the TSI. If the event is rejected (L1R), the data are discarded by not being stored. A Level 1 accept (L1A) comes with a 2-bit address which tells the board which of 4 buffers the data should be stored in. At some later time, if L2 rejects the event, no buffer readout instruction is sent and the buffer can be overwritten on a subsequent L1A[4]. If L2 accepts the event, the contents of that buffer may be read out over VME using block transfers by the DAQ.

There are two L2A datastream readout modes. In the normal mode, only the two 10-bit energy summaries for the two wedges and the 20-bit trigger summary are read out over VME using block transfers by the DAQ. In the trigger diagnostic readout mode, the original $\sum^{\mathrm{DIRAC}} \mathrm{E_T}$ and trigger summary words from each DIRAC are also read out after the CrateSum energy and trigger summary results.

3 CrateSum Input and Output Connectors

The front panel and backplane connectors and their functions are summarized in Table 5.

3.1 Front Panel Connectors

CrateSum has two front panel connectors[5], labeled CS-FR1 and CS-FR2, which deliver the two wedge energy and trigger summaries, respectively, to the Aux-cards [12] in the Global Level 1 crate. The Aux-cards translate the differential input data signals into individual signals directly usable by PreFRED and also place these bits on the custom backplane where they are available to PreFRED.

Table 6 lists the signals output from CS-FR1 and CS-FR2. For the purposes of this document, "Wedge 0" will refer to the ϕ wedge represented by the set of four DIRACs to the immediate left of the CS board when looking at the VME crate face-on. Likewise, "Wedge 1" will refer to the set on the right. Note that this definition of the wedges is NOT that used in the PreFRED specification [7].

Tables 7 and 8 list the pin assignments for the CS-FR1 and CS-FR2 connectors. The CS-FR1 connector sends out the two 10-bit $\sum^{\mathrm{Wedge}} \mathrm{E_T}$ words, one for each wedge, in two sequential steps of 66 ns each, on the same data lines[6]. PreFRED requires either the Wedge 0 or Wedge 1 $\mathrm{E_T}$ word to be sent first, depending on the particular CrateSum board involved.

[4]Note that CrateSum does not keep track of which buffers are full, nor the results of any decision. If the TSI tells CrateSum to put an event in a given buffer, CS simply assumes that that buffer is free for writing.

[5]20-pin SCSI-II type connectors are used.

[6]This procedure halves the number of required lines, thus allowing the use of 20-pin connectors rather than the high-density 40-pin ones originally considered.

Please refer to the PreFRED specification [7] for details. The status of a 1-bit "parity" register on CrateSum determines which wedge energy summary is output first. The value of this bit must be downloaded before the beginning of a run. The CS-FR2 connector likewise sends out the trigger bit summary in two sequential words. The five double-bit trigger bits are sent in the first 66 ns and the ten single-bit trigger bits in the subsequent 66 ns. To prevent data corruption and decrease noise, differential signals are used to pass data from CrateSum to the Global Level 1 crate.

3.2 Backplane Connectors

CS-P1, CS-P2, and CS-P3 are the backplane connectors and connect to the J1, J2, and J3 backplanes, respectively. They are used for downloading, run-time interactions with the TSI, readout, diagnostics, and for receiving data from DIRAC. CS-P1 and CS-P2 are standard VMEbus connectors which are VME64 extension compatible. The user-defined pins on CS-P2 provide additional power and ground beyond the VME standard, as well as pass along signals from the TSI. Table 9 lists the signals generated by the TSI and Table 10 shows the pin connections for CS-P2. The CS-P3 connector[7] receives energy and trigger data from the DIRACs. Table 11 lists the data bits from DIRAC and Table 12 lists the pin assignments on CS-P3. Note that if a DIRAC is not plugged in, CrateSum considers the input from that card to consist of all zeroes.

4 Dataflow

4.1 Clocking Data Through CrateSum

During the following discussion, reference will be made to several different sections of the CrateSum board. A functional schematic of the dataflow appears as Figure 4.

The flow of data on CrateSum is regulated by a number of 132ns period clock signals output by the **CONTROL**. Data processing on CrateSum (CS) begins when a run starts. The sequence is initiated by a series of signals from the TSI [9]. First the TSI asserts HALT and then asserts RECOVER[8]. CrateSum then begins processing events after the next B0 signal. After receiving the B0 signal, **CONTROL** issues signals at times $T_{\mathrm{P3LatchET}}$ and $T_{\mathrm{P3LatchTrig}}$ after B0 to latch in the energy and trigger bit information from the CS-P3 connector into the **P3 Latch** section. Since the trigger and energy summaries may arrive at different times and be from different events, separate signals are sent for each. However, it is assumed that all eight DIRAC summaries are available at the CS-P3 connector simultaneously. After the data has been latched in, it then becomes available for processing. The next few paragraphs describe the dynamics of processing the data and clocking it through the remainder of the board.

The half-crate energy summary is performed by two identical subsections in **Energy Summary**. Each of these subsections receives the four 8-bit $\overset{\mathrm{DIRAC}}{\Sigma}\ \mathrm{E_T}$ words from a single

[7]CS-P3 is a 220 pin 2mm hard metric (e.g. AMP Z-pack) connector with 5 columns of 44 pins each.

[8]Recall that these signals, as well as most of the other signals on P2, are TTL levels and are active low.

ϕ wedge and sums them into a single 10-bit word, $\sum^{\text{Wedge}} \mathrm{E_T}$. The **Trigger Summary** takes in the eight 16-bit trigger summaries from the **P3 Latch** and performs the 20-bit half-crate summary. After the summaries of the energy and trigger are completed, they are latched. The latching clock signals (which are perhaps more properly to be regarded as "strobes") begin at times $\Delta T_{\text{proclatchET}}$ for the energy summary and $\Delta T_{\text{proclatchTrig}}$ for the trigger bit summary. These times are defined relative to the times $T_{\text{P3LatchET}}$ and $T_{\text{P3LatchTrig}}$, respectively. The energy and trigger bit summary and latching are performed by an Altera FLEX10K70 PLD.

After being latched in the processor chip, the summarized data is clocked into FIFOs starting at times $\Delta T_{\text{L1FIFOETSum}}$ and $\Delta T_{\text{L1FIFOTrigSum}}$. The first data into each empty FIFO chip is immediately available at the FIFO's output registers. At some later time, the board will begin to receive L1 Decision signals. If a L1A is detected, the data event it is for will be read out and stored in a buffer whose location is specified by the buffer address accompanying the L1A signal. Otherwise, receipt of a L1R signal will cause the corresponding data to be clocked out of the FIFO but not written to any buffer.

It is not only the summarized $\mathrm{E_T}$ and trigger data that are stored in FIFOs and buffers. Beginning at times $\Delta T_{\text{L1FIFOETRaw}}$ and $\Delta T_{\text{L1FIFOTrigRaw}}$, the raw DIRAC $\sum^{\text{DIRAC}} \mathrm{E_T}$ and trigger bit words received by CrateSum on the backplane are clocked into FIFOs. This data is stored into buffers or clocked out and not stored, depending on the receipt of L1A or L1R signals.

Data stored in the buffers may be read out at some later time through the VME. In the trigger diagnostic readout mode, the datastream contains both summarized and raw DIRAC data, whereas in the normal readout mode, only the summed data is present. In either mode, all words are readout in a single block transfer.

4.2 CrateSum Control Registers

Only the times $T_{\text{P3LatchET}}$ and $T_{\text{P3LatchTrig}}$ need to be downloaded before a run begins. The Controller chip has a bank of registers for the purpose of storing this timing information. Table 2 lists each register and its access mode type and VME address. All registers which have writeable access modes ("W") must be downloaded before the beginning of a run.

The B0_offset_ET(5:0) register, a 6-bit register, stores the number of 132ns CDF_CLK cycles after the receipt of the B0 signal before CrateSum gets valid E_T data for the first event ("Bunch 0") from DIRAC on the P3 backplane. (This number can be any integer value between 1 and 64 in theory, although the number determined at the conclusion of system integration will be less than 41.) Likewise, the B0_offset_Trig(5:0) register stores the number of 132ns CDF_CLK cycles after B0 before CrateSum gets trigger data from DIRAC on P3.

CrateSum tap-delays the CDF_CLK signal it receives into 6 individual clock lines (CDF_CLK(5:0)), each consecutive line delayed by an incrementing multiple of 22ns, beginning with zero. The DIRAC_ET_delay(2:0) 3-bit register picks one of these 6 clock signals. The time $T_{\mathrm{P3LatchET}}$ is then determined as the rising edge of the CDF_CLK(5:0) signal specified by DIRAC_ET_delay(2:0) in the particular CDF_CLK cycle indicated by B0_offset_ET(5:0). In other words, E_T data from P3 is latched on the rising edge of the CDF_CLK(5:0) clock (picked by DIRAC_ET_delay(2:0)) in the 132ns period CDF_CLK multiple (indicated in B0_offset_ET(2:0)). The DIRAC_Trig_delay(2:0) register serves the same purpose as DIRAC_ET_delay(2:0), except that it is for trigger data rather than E_T.

One can think of the B0_offset_ET(Trig) register as a coarse adjustment knob for the time $T_{\mathrm{P3LatchET}}$ ($T_{\mathrm{P3LatchTrig}}$) (in units of 132ns) after the assertion of B0. The DIRAC_ET(Trig)_delay is a fine adjustment tuning knob for this time.

As previously stated, only the times $T_{\mathrm{P3LatchET}}$ and $T_{\mathrm{P3LatchTrig}}$ need to be downloaded before a run begins. In the interest of clarity, it is stated here that $\Delta T_{\mathrm{proclatchET}}$, $\Delta T_{\mathrm{L1FIFOETSum}}$, and $\Delta T_{\mathrm{L1FIFOETRaw}}$, as well as the corresponding "ΔT"s for the trigger data, are not stored in downloadable registers. Their values are all "fixed" in the internal logic of the Controller Altera PLD, and have been selected to allow sufficient time for data to be summarized (in the case of $\Delta T_{\mathrm{proclatchET}}$), and for raw and summed data to be valid at the inputs of the appropriate L1FIFOs (for $\Delta T_{\mathrm{L1FIFOETSum}}$ and $\Delta T_{\mathrm{L1FIFOETRaw}}$, respectively). These times are based on the 22ns-delayed CDF_CLK(5:0) signals. Table 3 shows the approximate values of these times.

4.3 DAQ and TSI Interactions

4.3.1 Readout Interactions

As previously mentioned, the half-crate energy and trigger summaries must be stored until they are either discarded or read out into the data stream. This is done in the two-stage process shown in Figure 5. The half-crate summaries for each event are first latched into a FIFO, which stores the data until it receives a L1 decision from the TSI[9]. If the event is rejected (L1R), the data are thrown away (i.e. clocked out of the FIFO and never stored anywhere). If it is accepted (L1A), the data are stored in the buffer specified by the address signals L2B0 and L2B1 which come along with the L1A. If L2 rejects the event, no signal is sent and the buffer is overwritten on a subsequent L1A. If L2 accepts the event, the event

[9] Note that since the energy and trigger summaries come at different times, latching the data into the FIFO occurs at different times. However, only a single clock out is required since the summaries are aligned by the FIFO.

CrateSum Control Registers

Word[bit]	Name	Access	VME Address	Description
0[5:0]	B0_offset_ET[5:0]	R/W	0x000000	Bunch 0 E_T offset in 132ns units
1[5:0]	B0_offset_Trig[5:0]	R/W	0x000004	Bunch 0 Trig offset in 132ns units
2[2:0]	DIRAC_ET_delay[2:0]	R/W	0x000008	Fine delay in increments of 22ns to latch in E_T data from P3
2[5:3]	DIRAC_Trig_delay[2:0]	R/W	”	Fine delay in increments of 22ns to latch in Trig data from P3
3[0]	run	R/W	0x00000C	Mode of operation: 1=run; 0=load
3[1]	recover	R/W	”	When asserted (=1) in load mode, resets the L1FIFOs and the board error bit
3[2]	FIFO_Rclk	R/W	”	When set to 1 in load mode, generates a strobe that reads out the L1FIFOs
3[3]	L2B_W	R/W	”	When set to 1 in load mode, generates a strobe to write to a DAQ buffer
3[5:4]	L2B[1:0]	R/W	”	In load mode, the DAQ buffer address to write to when L1B_W is asserted
4[7:0]	Mask_DIRAC[7:0]	RO	0x000010	DIRAC masking bits
5[1:0]	ET_Sum_FF_Mask[1:0]	RO	0x000014	E_T Sum Full FIFO flag masks
5[3:2]	Trig_Sum_FF_Mask[1:0]	RO	”	Trig Sum Full FIFO flag masks
5[7:4]	ET_Raw_FF_Mask[3:0]	RO	”	E_T Raw Full FIFO flag masks
6[7:0]	Trig_Raw_FF_Mask[7:0]	RO	0x000018	E_T Raw Full FIFO flag masks
7[1:0]	FF_ET_Sum[1:0]	RO	0x00001C	E_T Sum Full FIFO flags
7[3:2]	FF_Trig_Sum[1:0]	RO	”	Trig Sum Full FIFO flags
7[7:4]	FF_ET_Raw[3:0]	RO	”	E_T Raw Full FIFO flags
8[7:0]	FF_Trig_Raw[7:0]	RO	0x000020	Trig Raw Full FIFO flags
9[1:0]	EF_ET_Sum[1:0]	RO	0x000024	E_T Sum Empty FIFO flags
9[3:2]	EF_Trig_Sum[1:0]	RO	”	Trig Sum Empty FIFO flags
9[7:4]	EF_ET_Raw[3:0]	RO	”	E_T Raw Empty FIFO flags
10[7:0]	EF_Trig_Raw[7:0]	RO	0x000028	Trig Raw Empty FIFO flags
11[0]	_P3_Latch_OE	R/W	0x00002C	When set to 0, P3 Latch is enabled; when set to 1, P3 Latch is disabled
11[1]	src_data	R/W	”	When =0, indicates data is from P3; when =1, indicates data is fake VME input
11[2]	Bunch_Ctr_FF_Mask	R/W	”	Bunch Counter Full FIFO flag mask
12[0]	proc_latch_clk_ET	R/W	0x000030	When set to 1 in load mode, generates a strobe that that enables the processor to latch processed E_T data
12[1]	L1FIFO_Wclk_ET_Sum	R/W	”	When set to 1 in load mode, generates a strobe to latch data into the E_T Sum L1FIFOs
12[2]	proc_latch_clk_Trig	R/W	”	When set to 1 in load mode, generates a strobe that that enables the processor to latch processed Trig data
12[3]	L1FIFO_Wclk_Trig_Sum	R/W	”	When set to 1 in load mode, generates a strobe to latch data into the Trig Sum L1FIFOs
12[4]	P3_Latch_clk_ET	R/W	”	When set to 1 in load mode, allows P3 Latch to latch DIRAC E_T data from P3
12[5]	P3_Latch_clk_Trig	R/W	”	When set to 1 in load mode, allows P3 Latch to latch DIRAC Trig data from P3
12[6]	L1FIFO_Wclk_ET_Raw	R/W	”	When set to 1 in load mode, generates a strobe to latch data into the E_T Raw L1FIFOs
12[7]	L1FIFO_Wclk_Trig_Raw	R/W	”	When set to 1 in load mode, generates a strobe to latch data into the Trig Raw L1FIFOs
13[0]	parity	R/W	0x000034	When =0, Wedge 0 E_T summary is output first on FP; when =1, Wedge 1 output first
13[1]	board_error	RO	”	Board error bit; is set when any Full FIFO flag is set, unless the flag is masked
13[2]	FF_Bunch_Ctr	RO	”	Bunch Counter Full FIFO flag
13[3]	EF_Bunch_Ctr	RO	”	Bunch Counter Empty FIFO flag
14[7]	src_config	RO	0x000038	Source configuring the FLEX10K devices: 0 = EPROMS; 1 = download cable
14[6:0]	ctrl_version[6:0]	RO	”	Controller version number
15[7:0]	proc_version[7:0]	RO	0x00003C	Processor version number

Table 2: CrateSum control registers. These are 8-bit words which map the 8 MSB of the VME 32-bit data bus. Bits which have no function specified can be used as spare bits.

ΔT Values

Name	Approximate Value in ns
$\Delta T_{\mathrm{L1FIFOETRaw}}$	22
$\Delta T_{\mathrm{proclatchET}}$	66
$\Delta T_{\mathrm{L1FIFOETSum}}$	132
$\Delta T_{\mathrm{L1FIFOTrigRaw}}$	22
$\Delta T_{\mathrm{proclatchTrig}}$	66
$\Delta T_{\mathrm{L1FIFOTrigSum}}$	132

Table 3: The values of the various ΔTs for clocking data through CrateSum.

is read out using VME block transfers. The VMEbus addresses for these, as well as other, VME transfers are listed in Table 4.

VME Address Map for CrateSum

Name	Port location	Access	VME Address (A23:A0)	Description
Control registers	Control	R/W	0x000038:0x000000	
Module ID	Control	RO	0x10007C:0x100000	Module ID ASCII word
E_T data from VME	Control/Processor	WO	0x200000 0x200004	Wedge 0 Wedge 1
Trig data from VME	Control/Processor	WO	0x300000 0x300004 0x300008 0x30000C	Quarter 1 Quarter 2 Quarter 3 Quarter 4
Processor readout via VME	Processor	RO	0x400000 0x400004 0x400008 0x40000C 0x400010 0x400014 0x400018 0x40001C	ET_Raw Wedge 0 ET_Raw Wedge 1 Trig_Raw Quarter 1 Trig_Raw Quarter 2 Trig_Raw Quarter 3 Trig_Raw Quarter 4 ET_Sum Trig_Sum
Bunch Counter value from VME	Controller	WO	0x500000	
L2 Buffer 0	DAQ Buffer 0	RO	0x800020: 0x800000	
L2 Buffer 1	DAQ Buffer 1	RO	0x900020: 0x900000	
L2 Buffer 2	DAQ Buffer 2	RO	0xA00020: 0xA00000	
L2 Buffer 3	DAQ Buffer 3	RO	0xB00020: 0xB00000	

Table 4: VME address map for CrateSum. A1 and A0 are both zero because CDF uses full 32-bit (quad word) data transfers.

In the standard VME crate, only 32-bit VMEbus addressing and data transfers will be used. The two single-wedge energy summaries are grouped as one word and the trigger summary as a separate word. Both words are read out in a single block transfer while in normal readout mode. These words are followed by the DIRAC $\overset{\mathrm{DIRAC}}{\Sigma} E_T$ and trigger P3 data in the trigger diagnostic readout mode. The first word of the datastream is the board header word, which reports the bunch counter value of the event, the board serial number, and the board type. See [16] for details.

4.3.2 Diagnostics

In order to perform a full set of diagnostics, it is necessary to be able to write to and read from most places on the board, including databuses. Several diagnostic features have been incorporated in the design of the board. Included, in particular, is an especially important diagnostic test feature that allows fake E_T and/or Trig data to be sent to the data input ports of the processor via a VME write instruction to the appropriate "E_T data from VME" or "Trig data from VME" address (see Table 4). A strobe to latch the summed data inside the processor can be issued, and a subsequent VME read from the "Processor readout via VME" addresses will return the input fake data along with the summaries. This diagnostic is capable of ascertaining whether or not the processor is performing correctly.

Another step-by-step test, involving the processor as well as the L1FIFOs and the buffers, can be performed. Again, fake E_T and/or Trig data is sent to the processor via the VME. Sequential strobes are then issued to latch the summed data inside the processor and to write the raw fake and summed data into the appropriate L1FIFOs. This data can be written to a buffer by issuing buffer write strobes (as well as L1FIFO read commands, as necessary). The data is read out by issuing VME read commands targeting the correct buffer.

4.4 Error Handling/Board Status

CrateSum has two complementary operational modes: load and run. Downloading and most diagnostics require the board to be in the load mode. A register in the Controller Altera PLD stores the mode information. Since downloading of all writeable registers is required upon board start-up and before beginning a run, the Controller has been designed to start up in the load mode. This feature has been incorporated in the design, not to obviate the need to download the operational mode bit at start-up (since the state of writeable registers should never be assumed without having previously written to them), but rather as a precaution in the event that this mode bit is not downloaded before attempting to write to other registers.

The Controller also stores the status of an error bit, called "board_error". This bit goes high if the full flag of any FIFO on the board is asserted, unless this flag is ignored because its full FIFO masking bit is set. The error bit is placed on CS-P2 and is detected by the TRACER. Diagnostics, including VME instructions to read all FIFO full flags, must be run in order to study any errors and their origins. See Reference [17] for further details.

Connector	Description
CS-FR1	Front panel connector used to send out energy signals from CS to PreFRED.
CS-FR2	Front panel connector used to send out trigger signals from CS to PreFRED.
CS-P1	VME J1 backplane connector. Passes VME instructions and data.
CS-P2	VME J2 backplane connector. Used for VME and TSI interactions.
CS-P3	Custom J3 backplane connector. Passes DIRAC E_T and trigger data to CS.

Table 5: List of CrateSum front panel and backplane connectors. Note that the P0 connector on the backplane is not used by CrateSum.

Signal Name	Description
ET_PHI0(9)	Most Significant Bit, $\sum^{\text{Wedge}} E_T$ 0th wedge
ET_PHI0(8)	Next to Most Significant Bit, $\sum^{\text{Wedge}} E_T$ 0th wedge
⋮	⋮
ET_PHI0(1)	Next to Least Significant Bit, $\sum^{\text{Wedge}} E_T$ 0th wedge
ET_PHI0(0)	Least Significant Bit, $\sum^{\text{Wedge}} E_T$ 0th wedge
ET_PHI1(9)	Most Significant Bit, $\sum^{\text{Wedge}} E_T$ 1st wedge
ET_PHI1(8)	Next to Most Significant Bit, $\sum^{\text{Wedge}} E_T$ 1st wedge
⋮	⋮
ET_PHI1(1)	Next to Least Significant Bit, $\sum^{\text{Wedge}} E_T$ 1st wedge
ET_PHI1(0)	Least Significant Bit, $\sum^{\text{Wedge}} E_T$ 1st wedge
TRIG(0)	Trigger Bit 0
TRIG(1)	Trigger Bit 1
TRIG(2)	Trigger Bit 2
⋮	⋮
TRIG(18)	Trigger Bit 18
TRIG(19)	Trigger Bit 19

Table 6: CrateSum output signal names. "Wedge 0" corresponds to the set of four DIRACs to the left of a particular CrateSum board and "Wedge 1" to the four boards to the right.

Pin	Signal, Cycle 1	Pin	Signal, Cycle 1	Pin	Signal, Cycle 2	Pin	Signal, Cycle 2
1	ET_PHIA(0)	2	$\overline{\text{ET\_PHIA(0)}}$	1	ET_PHIB(0)	2	$\overline{\text{ET\_PHIB(0)}}$
3	ET_PHIA(1)	4	$\overline{\text{ET\_PHIA(1)}}$	3	ET_PHIB(1)	4	$\overline{\text{ET\_PHIB(1)}}$
5	ET_PHIA(2)	6	$\overline{\text{ET\_PHIA(2)}}$	5	ET_PHIB(2)	6	$\overline{\text{ET\_PHIB(2)}}$
7	ET_PHIA(3)	8	$\overline{\text{ET\_PHIA(3)}}$	7	ET_PHIB(3)	8	$\overline{\text{ET\_PHIB(3)}}$
9	ET_PHIA(4)	10	$\overline{\text{ET\_PHIA(4)}}$	9	ET_PHIB(4)	10	$\overline{\text{ET\_PHIB(4)}}$
11	ET_PHIA(5)	12	$\overline{\text{ET\_PHIA(5)}}$	11	ET_PHIB(5)	12	$\overline{\text{ET\_PHIB(5)}}$
13	ET_PHIA(6)	14	$\overline{\text{ET\_PHIA(6)}}$	13	ET_PHIB(6)	14	$\overline{\text{ET\_PHIB(6)}}$
15	ET_PHIA(7)	16	$\overline{\text{ET\_PHIA(7)}}$	15	ET_PHIB(7)	16	$\overline{\text{ET\_PHIB(7)}}$
17	ET_PHIA(8)	18	$\overline{\text{ET\_PHIA(8)}}$	17	ET_PHIB(8)	18	$\overline{\text{ET\_PHIB(8)}}$
19	ET_PHIA(9)	20	$\overline{\text{ET\_PHIA(9)}}$	19	ET_PHIB(9)	20	$\overline{\text{ET\_PHIB(9)}}$

Table 7: Pin assignments for CS-FR1. Cycle 1 refers to the first 66 ns interval of a data cycle, and Cycle 2 refers to the second. A is 0 or 1 and B is 1 or 0 depending on the state of the "parity" register.

Pin	Signal, Cycle 1	Pin	Signal, Cycle 1	Pin	Signal, Cycle 2	Pin	Signal, Cycle 2
1	TRIG(0)	2	$\overline{\text{TRIG(0)}}$	1	TRIG(10)	2	$\overline{\text{TRIG(10)}}$
3	TRIG(1)	4	$\overline{\text{TRIG(1)}}$	3	TRIG(11)	4	$\overline{\text{TRIG(11)}}$
5	TRIG(2)	6	$\overline{\text{TRIG(2)}}$	5	TRIG(12)	6	$\overline{\text{TRIG(12)}}$
7	TRIG(3)	8	$\overline{\text{TRIG(3)}}$	7	TRIG(13)	8	$\overline{\text{TRIG(13)}}$
9	TRIG(4)	10	$\overline{\text{TRIG(4)}}$	9	TRIG(14)	10	$\overline{\text{TRIG(14)}}$
11	TRIG(5)	12	$\overline{\text{TRIG(5)}}$	11	TRIG(15)	12	$\overline{\text{TRIG(15)}}$
13	TRIG(6)	14	$\overline{\text{TRIG(6)}}$	13	TRIG(16)	14	$\overline{\text{TRIG(16)}}$
15	TRIG(7)	16	$\overline{\text{TRIG(7)}}$	15	TRIG(17)	16	$\overline{\text{TRIG(17)}}$
17	TRIG(8)	18	$\overline{\text{TRIG(8)}}$	17	TRIG(18)	18	$\overline{\text{TRIG(18)}}$
19	TRIG(9)	20	$\overline{\text{TRIG(9)}}$	19	TRIG(19)	20	$\overline{\text{TRIG(19)}}$

Table 8: Pin assignments for CS-FR2. Cycle 1 refers to the first 66 ns interval of a data cycle, and Cycle 2 refers to the second. TRIG(0) through TRIG(9) refer to the five 2-bit trigger bits and TRIG(10) through TRIG(19) refer to the ten single-bit trigger bits.

Signal Name	Description	Used by CS?
CLK	Differential PECL Clock signal (132ns)	**Yes**
CLK*	Differential PECL Clock signal (132ns)	**Yes**
BC*	Bunch Crossing	No
B0*	Bunch 0	**Yes**
L1A*	Global Level 1 Accept Signal	**Yes**
L1R*	Global Level 1 Reject Signal	**Yes**
L2B0*	Level 1 Accept Buffer Address 0	**Yes**
L2B1*	Level 1 Accept Buffer Address 1	**Yes**
HALT*	Stop filling L1 FIFO/pipelines and processing events.	**Yes**
RECOVER*	Master Reset; Reset FIFOs and Pipelines	**Yes**
ABORT*	Dump Everything	No
CALIB0*	Calibration bit 0	No
⋮	⋮	⋮
CALIB6*	Calibration bit 6	No
CALEN*	Calibration Enable	No
ERROR*	Error bit sent to TSI in the event of an error in the L1 Crate.	**Yes**
L2A*	Global Level 2 Accept Signal	No
L2R*	Global Level 2 Reject Signal	No
L2A_EN*	L2 Accept Enable Signal	No
L2BD0*	L2 Accept Decision Buffer Address Bit 0	No
L2BD1*	L2 Accept Decision Buffer Address Bit 1	No
RSVD0*	Reserved bit	No
RSVD1*	Reserved bit	No
TDC_CAL0*	TDC Calibration Pulses produced by the TRACER.	No
TDC_CAL1*	TDC Calibration Pulses produced by the TRACER.	No
TDC_CAL2*	TDC Calibration Pulses produced by the TRACER.	No
TDC_CALIB	Precision TDC Calibration Pulse	No
TDC_CALIB*	Precision TDC Calibration Pulse	No
TDC_DONE*	Indicates that TDCs have moved data into local L2 buffers.	No
GLIVE*	L1 Accept corresponds to live Beam Crossing	No
RSVD_L1W1*	TSI reserved L1 word bit(7)	No
RSVD_L1W2*	TSI reserved L1 word bit(8)	No
STOP*	Set Halt Condition	No
TEST*	Diagnostic Bit	No
RUN*	Clear Halt Condition	No
RL0*	Readout List Identifier bit	No
RL1*	Readout List Identifier bit	No
RL2*	Readout List Identifier bit	No
EVID0*	Event Identifier bit 0	No
EVID1*	Event Identifier bit 1	No
EVID2*	Event Identifier bit 2	No
EVID3*	Event Identifier bit 3	No

Table 9: Signals sent from the Trigger System Interface along CS-P2. Signal names are preceeded by the prefix "CDF_". All signals are TTL levels and active low, with the exception of CLK, CLK*, TDC_CALIB, and TDC_CALIB* (differential PECL) and ERROR and TDC_DONE (open collector). Details can be found in CDF Note 2388 (July 1997).

PIN	Row					Comments
	z	A	B	C	d	
1	V	Term Usr Bus		TDC_CAL0*	V	
2	M	Term Usr Bus		TDC_CAL1*	M	
3	E	Term Usr Bus		TDC_CAL2*	E	
4	6	Term Usr Bus		TDC_CALIB	6	(CMOS)
5	4	Term Usr Bus	S	TCD_CALIB*	4	
6		CLK	T	TDC_DONE		132ns (7 RF Bucket) Clock
7	E	CLK*	A	Term Usr Bus	E	DIFF (PECL)
8	x	Term Usr Bus	N	Term Usr Bus	x	
9	t	BC*	D	Term Usr Bus	t	Beam Crossing Indicator (TTL Active Low)
10	e	B0*	A	Term Usr Bus	e	Bunch 0 Indicator (TTL Active Low)
11	n	Term Usr Bus	R	Term Usr Bus	n	
12	s	L1A*	D	GLIVE*	s	L1 Accept (TTL Active Low)
13	i	L1R*		L1W1*	i	L1 Reject (TTL Active Low)
14	o	L2B0*		L2W2*	o	L1A buffer address 0 (TTL Active Low)
15	n	L2B1*		STOP*	n	L1A buffer address 1 (TTL Active Low)
16	s	HALT*		TEST*	s	Halt Filling L1 Pipeline
17		Term Usr Bus	V	RUN*		
18	S	RECOVER*	M	RL0*	S	Reset FIFOs/Buffers (TTL Active Low)
19	t	Term Usr Bus	E	RL1*	t	
20	a	ABORT*	b	RL2*	a	Abort Gap starting (TTL Active Low)
21	n	CALIB0*	u	CALIB3*	n	Calibration enable 0 (TTL Active Low)
22	d	Term Usr Bus	s	CALIB4*	d	
23	a	CALIB1*		CALIB5*	a	Calibration enable 1 (TTL Active Low)
24	r	CALIB2*		CALIB6*	r	Calibration enable 2 (TTL Active Low)
25	d	Term Usr Bus		CALEN*	d	
26		ERROR*		Term Usr Bus		Error on card (Output OC TTL)
27	P	L2A*		L2R*	P	L2 Accept (TTL Active Low)
28	i	L2BD0*		L2A_EN*	i	L2A Buffer Address 0 (TTL Active Low)
29	n	Term Usr Bus		EVID0*	n	
30	o	L2BD1*		EVID1*	o	L2A Buffer Address 1 (TTL Active Low)
31	u	RSVD0*		EVID2*	u	
32	t	RSVD1*		EVID3*	t	

Table 10: Pin assignments for the Standard VME CS-P2 connector to the J2 Backplane. The pin assignments are taken directly from CDF Note 2388 (July 1997). Rows z and d follow the VME64 Extensions Standard Pinout specification. The middle row, Row B, is dedicated for standard VMEbus signals. Rows A and C are used to distribute timing signals from the TRACER. All “Term Usr Bus” lines in rows A and C are reserved. They are terminated in the same way that VMEbus address/data lines are.

Signals sent from DIRAC

Signal Name	Description
ETSUM(7)	E_T Most Significant Bit
ETSUM(6)	E_T Next-to-Most Significant Bit
⋮	⋮
ETSUM(1)	E_T Next-to-Least Significant Bit
ETSUM(0)	E_T Least Significant Bit
TRSUM(15)	Trigger bit 15
TRSUM(14)	Trigger bit 14
TRSUM(13)	Trigger bit 13
TRSUM(12)	Trigger bit 12
⋮	⋮
TRSUM(3)	Trigger bit 3
TRSUM(2)	Trigger bit 2
TRSUM(1)	Trigger bit 1
TRSUM(0)	Trigger bit 0

Table 11: Signals passed from DIRAC to CrateSum along the J3 backplane.

Pin #	z	a	b	c	d	e	f
1	GND	TRSUM0(2)	TRSUM0(1)	TRSUM0(0)	TRSUM7(1)	TRSUM7(0)	GND
2	GND	TRSUM0(4)	TRSUM0(3)	GND	TRSUM7(3)	TRSUM7(2)	GND
3	GND	TRSUM0(7)	TRSUM0(6)	TRSUM0(5)	TRSUM7(5)	TRSUM7(4)	GND
4	GND	TRSUM0(9)	TRSUM0(8)	GND	TRSUM7(7)	TRSUM7(6)	GND
5	GND	TRSUM0(11)	TRSUM0(10)	TRSUM7(10)	TRSUM7(9)	TRSUM7(8)	GND
6	GND	TRSUM0(13)	TRSUM0(12)	GND	TRSUM7(12)	TRSUM7(11)	GND
7	GND	TRSUM0(15)	TRSUM0(14)	TRSUM7(15)	TRSUM7(14)	TRSUM7(13)	GND
8	GND	TRSUM1(2)	TRSUM1(1)	TRSUM1(0)	TRSUM6(1)	TRSUM6(0)	GND
9	GND	TRSUM1(4)	TRSUM1(3)	GND	TRSUM6(3)	TRSUM6(2)	GND
10	GND	TRSUM1(7)	TRSUM1(6)	TRSUM1(5)	TRSUM6(5)	TRSUM6(4)	GND
11	GND	TRSUM1(9)	TRSUM1(8)	GND	TRSUM6(7)	TRSUM6(6)	GND
12	GND	TRSUM1(11)	TRSUM1(10)	TRSUM6(10)	TRSUM6(9)	TRSUM6(8)	GND
13	GND	TRSUM1(13)	TRSUM1(12)	GND	TRSUM6(12)	TRSUM6(11)	GND
14	GND	TRSUM1(15)	TRSUM1(14)	TRSUM6(15)	TRSUM6(14)	TRSUM6(13)	GND
15	GND	TRSUM2(2)	TRSUM2(1)	TRSUM2(0)	TRSUM5(1)	TRSUM5(0)	GND
16	GND	TRSUM2(4)	TRSUM2(3)	GND	TRSUM5(3)	TRSUM5(2)	GND
17	GND	TRSUM2(7)	TRSUM2(6)	TRSUM2(5)	TRSUM5(5)	TRSUM5(4)	GND
18	GND	TRSUM2(9)	TRSUM2(8)	GND	TRSUM5(7)	TRSUM5(6)	GND
19	GND	TRSUM2(11)	TRSUM2(10)	TRSUM5(10)	TRSUM5(9)	TRSUM5(8)	GND
20	GND	TRSUM2(13)	TRSUM2(12)	GND	TRSUM5(12)	TRSUM5(11)	GND
21	GND	TRSUM2(15)	TRSUM2(14)	TRSUM5(15)	TRSUM5(14)	TRSUM5(13)	GND
22	GND	TRSUM3(2)	TRSUM3(1)	TRSUM3(0)	TRSUM4(1)	TRSUM4(0)	GND
23	GND	TRSUM3(4)	TRSUM3(3)	GND	TRSUM4(3)	TRSUM4(2)	GND
24	GND	TRSUM3(7)	TRSUM3(6)	TRSUM3(5)	TRSUM4(5)	TRSUM4(4)	GND
25	GND	TRSUM3(9)	TRSUM3(8)	GND	TRSUM4(7)	TRSUM4(6)	GND
26	GND	TRSUM3(11)	TRSUM3(10)	TRSUM4(10)	TRSUM4(9)	TRSUM4(8)	GND
27	GND	TRSUM3(13)	TRSUM3(12)	GND	TRSUM4(12)	TRSUM4(11)	GND
28	GND	TRSUM3(15)	TRSUM3(14)	TRSUM4(15)	TRSUM4(14)	TRSUM4(13)	GND
29	GND	GND	GND	GND	GND	GND	GND
30	GND	ETSUM3(1)	ETSUM3(0)	GND	ETSUM4(1)	ETSUM4(0)	GND
31	GND	ETSUM3(3)	ETSUM3(2)	GND	ETSUM4(3)	ETSUM4(2)	GND
32	GND	ETSUM3(5)	ETSUM3(4)	ETSUM4(6)	ETSUM4(5)	ETSUM4(4)	GND
33	GND	ETSUM3(7)	ETSUM3(6)	GND	ETSUM5(0)	ETSUM4(7)	GND
Connector Key (equivalent to 3 pins)							
34	GND	ETSUM2(1)	ETSUM2(0)	GND	ETSUM5(2)	ETSUM5(1)	GND
35	GND	ETSUM2(3)	ETSUM2(2)	GND	ETSUM5(4)	ETSUM5(3)	GND
36	GND	ETSUM2(6)	ETSUM2(5)	ETSUM2(4)	ETSUM5(6)	ETSUM5(5)	GND
37	GND	ETSUM1(0)	ETSUM2(7)	GND	ETSUM6(0)	ETSUM5(7)	GND
38	GND	ETSUM1(2)	ETSUM1(1)	GND	ETSUM6(2)	ETSUM6(1)	GND
39	GND	ETSUM1(4)	ETSUM1(3)	GND	ETSUM6(4)	ETSUM6(3)	GND
40	GND	ETSUM1(6)	ETSUM1(5)	ETSUM6(7)	ETSUM6(6)	ETSUM6(5)	GND
41	GND	ETSUM0(0)	ETSUM1(7)	GND	ETSUM7(1)	ETSUM7(0)	GND
42	GND	ETSUM0(2)	ETSUM0(1)	GND	ETSUM7(3)	ETSUM7(2)	GND
43	GND	ETSUM0(4)	ETSUM0(3)	GND	ETSUM7(5)	ETSUM7(4)	GND
44	GND	ETSUM0(7)	ETSUM0(6)	ETSUM0(5)	ETSUM7(7)	ETSUM7(6)	GND

Table 12: Pin assignments for the CrateSum P3 connector on the J3 Backplane. The number at the end of the signal name is the DIRAC within the half-crate from which the signal came. (See Figure 2.) The number in parentheses is the bit number with 0 as the least significant bit.

CONTROL(130:0)

Control()	Name	Description
0	run	1 = run mode; 0 = load mode
1	src_ctrl_config	0 = EPROMs; 1 = FLEX Download Cable
2	_recover_	recover and halt; output from controller
3	run_or_vme / _src_data	0 = VME/fake data; 1 = backplane DIRAC data
5	L1FIFO_Wclk_ET_Sum	ET_Sum FIFO write clock
6	L1FIFO_Wclk_Trig_Sum	Trig_Sum FIFO write clock
9	L1FIFO_Wclk_Bunch_Ctr	Bunch Counter FIFO write clock
11	L1FIFO_Rclk	FIFO read clock
15	proc_version_ren	Read enable for processor version number
17:16	_EF_ET_Sum(1:0)	ET_Sum FIFOs(1:0) Empty Flag
19:18	_FF_ET_Sum(1:0)	ET_Sum FIFOs(1:0) Full Flag
21:20	_EF_Trig_Sum(1:0)	Trig_Sum FIFOs(1:0) Empty Flag
23:22	_FF_Trig_Sum(1:0)	Trig_Sum FIFOs(1:0) Full Flag
27:24	_EF_ET_Raw(3:0)	ET_Raw FIFOs(3:0) Empty Flag
31:28	_FF_ET_Raw(3:0)	ET_Raw FIFOs(3:0) Full Flag
39:32	_EF_Trig_Raw(7:0)	Trig_Raw FIFOs(7:0) Empty Flag
47:40	_FF_Trig_Raw(7:0)	Trig_Raw FIFOs(7:0) Full Flag
48	_EF_Bunch_Ctr	Bunch Counter Empty Flag
49	_FF_Bunch_Ctr	Bunch Counter Full Flag
53:52	L2BD(1:0)	Read address B (L2BD1) and read address A (L2BD0)
55:54	L2B(1:0)	Write address B (L2B1) and write address A (L2B0)
56	_L2B_W	Buffer write enable
57	_L2BD_R0	Board ID and bunch counter value read enable
58	_L2BD_R1	ET_Sum read enable
59	_L2BD_R2	Trig_Sum read enable
60	_L2BD_R3	ET_Raw wedge 0 read enable (ET_Raw buffers 0-7)
61	_L2BD_R4	ET_Raw wedge 1 read enable (ET_Raw buffers 8-15)
62	_L2BD_R5	Trig_Raw(1:0) read enable (Trig_Raw buffers 0-7)
63	_L2BD_R6	Trig_Raw(3:2) read enable (Trig_Raw buffers 8-15)
64	_L2BD_R7	Trig_Raw(5:4) read enable (Trig_Raw buffers 16-23)
65	_L2BD_R8	Trig_Raw(7:6) read enable (Trig_Raw buffers 24-31)
70:66	serial_number(4:0)	Serial number indicated by the DIP switches
78:71	bunch_cnt(7:0)	Bunch number from bunch counter
79	_P3_Latch_OE	Output enable to latch raw DIRAC data in
80	P3_Latch_clk_ET	Clock to latch raw DIRAC ET data in
81	P3_Latch_clk_Trig	Clock to latch raw DIRAC Trig data in
82	L1FIFO_Wclk_ET_Raw_wedge0	Write ET_Raw wedge 0 clock
83	L1FIFO_Wclk_ET_Raw_wedge1	Write ET_Raw wedge 1 clock
84	L1FIFO_Wclk_Trig_Raw_qtr1	Write Trig_Raw quarter 1 clock
85	L1FIFO_Wclk_Trig_Raw_qtr2	Write Trig_Raw quarter 2 clock
86	L1FIFO_Wclk_Trig_Raw_qtr3	Write Trig_Raw quarter 3 clock
87	L1FIFO_Wclk_Trig_Raw_qtr4	Write Trig_Raw quarter 4 clock
90	proc_latch_clk_ET / et_run_clk	Latch summed ET data into processor
91	proc_latch_clk_Trig / trig_run_clk	Latch summed trigger data into processor
99:92	mask_DIRAC(7:0)	DIRAC board(7:0) input masking bits
100	one_or_two_bits0_0	Trig(7:0)(1:0) summing: 0 = 8*2-to-2; 1 = two 8-to-1
101	one_or_two_bits0_1	Trig(7:0)(3:2) summing
102	one_or_two_bits1_0	Trig(7:0)(5:4) summing
103	one_or_two_bits1_1	Trig(7:0)(7:6) summing
104	one_or_two_bits2_0	Trig(7:0)(9:8) summing
105	one_or_two_bits2_1	Trig(7:0)(11:10) summing
106	one_or_two_bits3_0	Trig(7:0)(13:12) summing
107	one_or_two_bits3_1	Trig(7:0)(15:14) summing
108	FPmux_ET	132ns signal used by controller for multiplexing ET data
109	FPmux_Trig	132ns signal used by controller for multiplexing Trig data
110	vme_clk_ET	Clock to latch VME ET data into the processor
111	vme_clk_Trig	Clock to latch VME trigger data into the processor
112	store_vme_wedge_sel	VME ET latch wedge selector
114:113	store_vme_qtr_sel(1:0)	VME Trig latch qtr selector
115	proc_out_write / write_to_vme	Enables processor write to VME data bus
118:116	proc_out_sel(2:0)	Select lines for VME data written by processor
124:119	config(5:0)	Lines used to configure the FLEX10K devices

Table 13: Bus signals used to distribute commands throughout the CS board. Any numbers not appearing in the list above are not used and are spare bits.

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[12] P. Wilson, *J3 Backplane and Transition Module (L1AUX) for the Level 1 Calorimeter Trigger Upgrade*, Trigger Note #92, Dec. 1997.

[13] H. Frisch and P. Wilson, *Trigger Tower Organization and Summing in* $\eta - \phi$ *Space for Run II and Beyond*, CDF Note 2045, July 1995.

[14] D. Amidei, *Useful Trigger Constants V 2.00*, Trigger Note #51, 1987.

[15] If there is significant physics motivation, CrateSum and DIRAC can be adapted to change the meaning or number of trigger bits. In particular, it is not required that the 20 trigger bit summary produced by CrateSum consist of ten 1-bit numbers and five 2-bit numbers. For example, CrateSum can be reprogrammed to output ten 2-bit numbers, twenty 1-bit numbers, etc. If more bits are needed from DIRAC, 32 bits of trigger information per event can be sent from DIRAC using multiplexing across the J3 backplane. In this case, these bits must be de-multiplexed in the **P3 Latch** section.

[16] K. Ohl, J. Wahl, and P. Wilson, *Specification of DAQ/Trigger Synchronization Checking Protocol and VME board Header word*, CDF Note 3145, May 1995.

[17] A. Amadon *et al.*, *Error Detection and Handling for the Calorimeter Trigger*, Trigger Note #98, Jan. 1998.

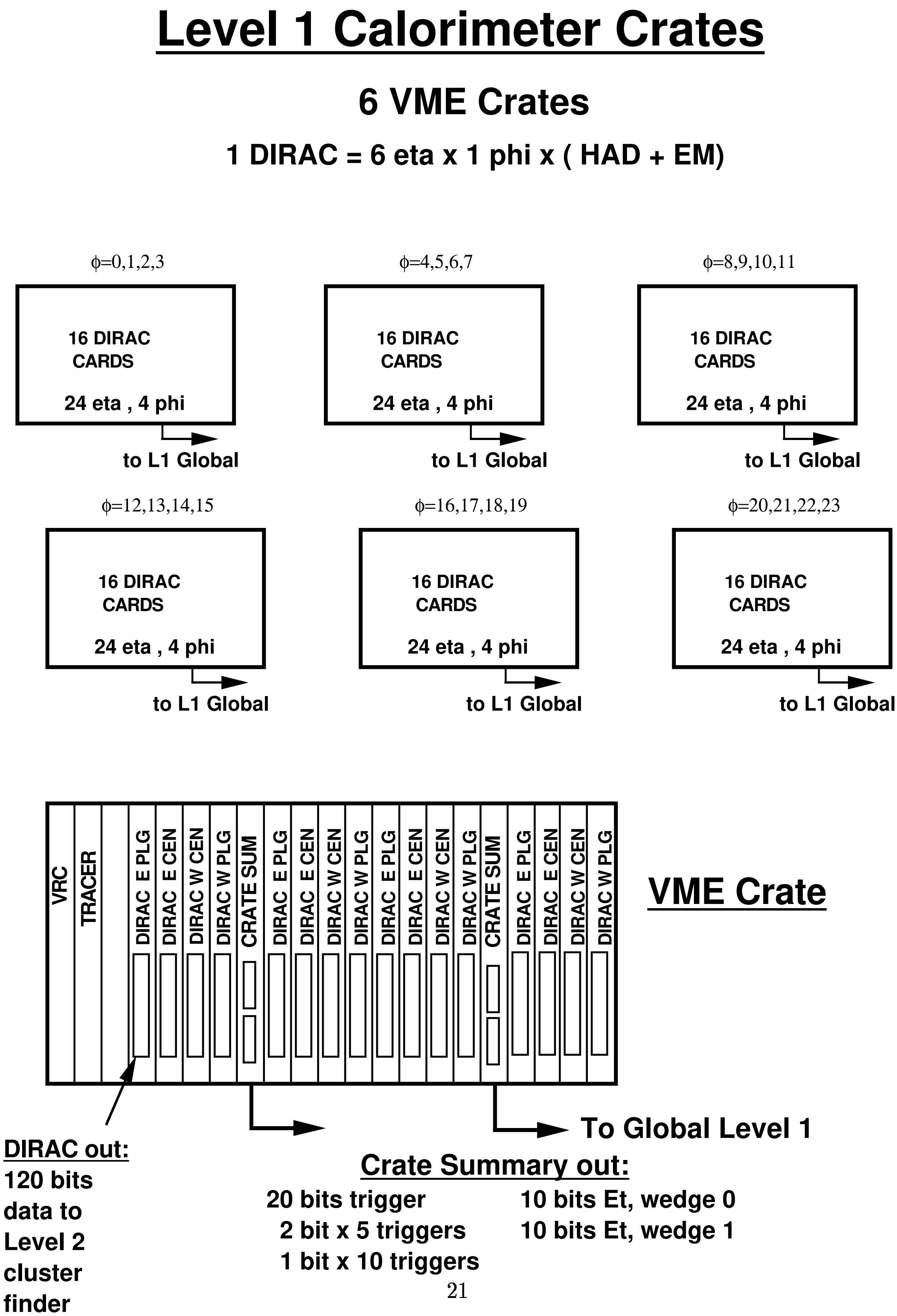

Figure 1: Physical Structure of the L1 Crate Layout.

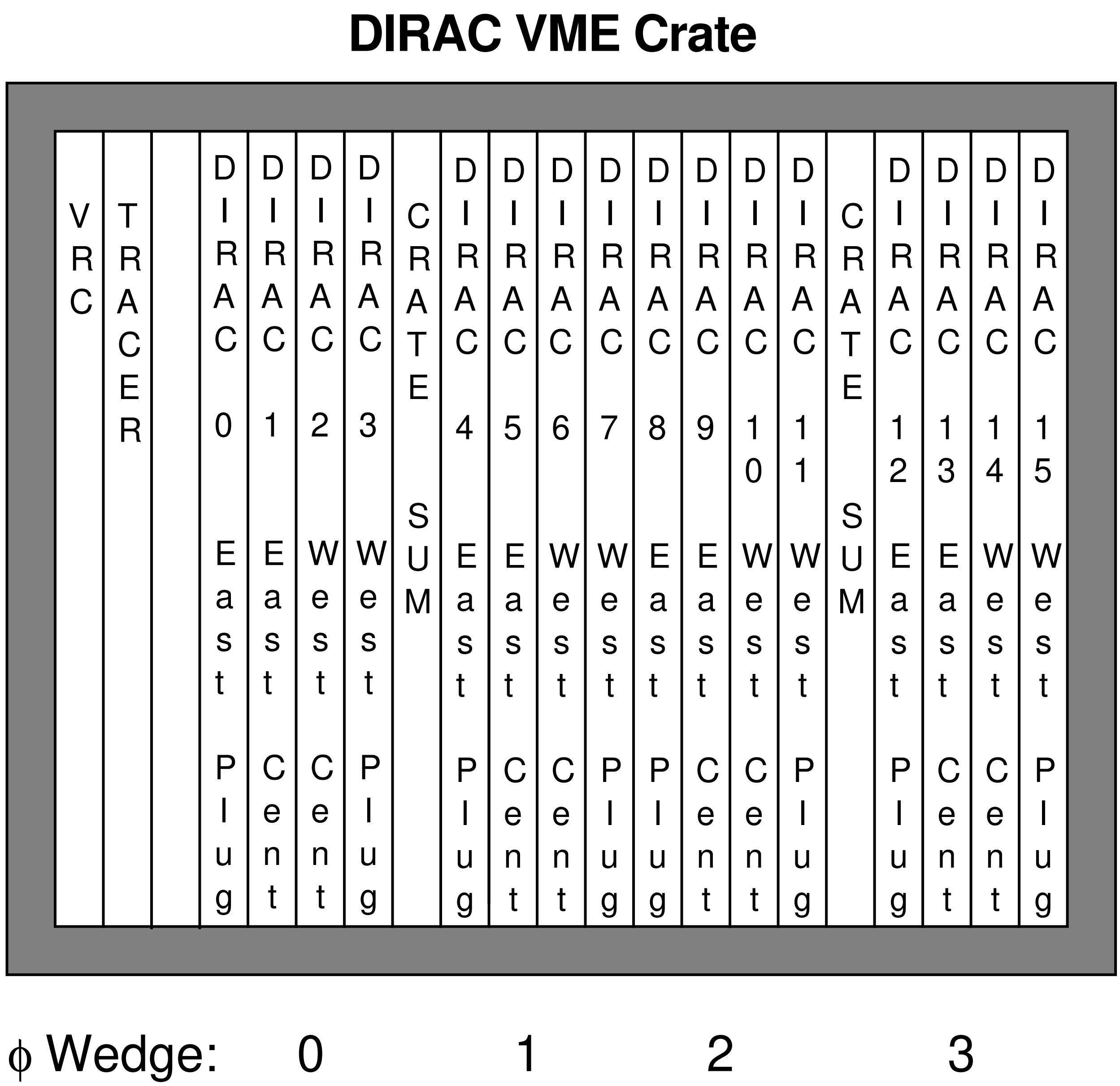

Figure 2: Physical Structure of the Crate. Note that this setup reflects the fact that the upgrade CAS equivalent will not lie in this crate as it is no longer used in a L1 decision. Also note that the CrateSum card is in the center of the eight DIRAC boards from which it accepts signals.

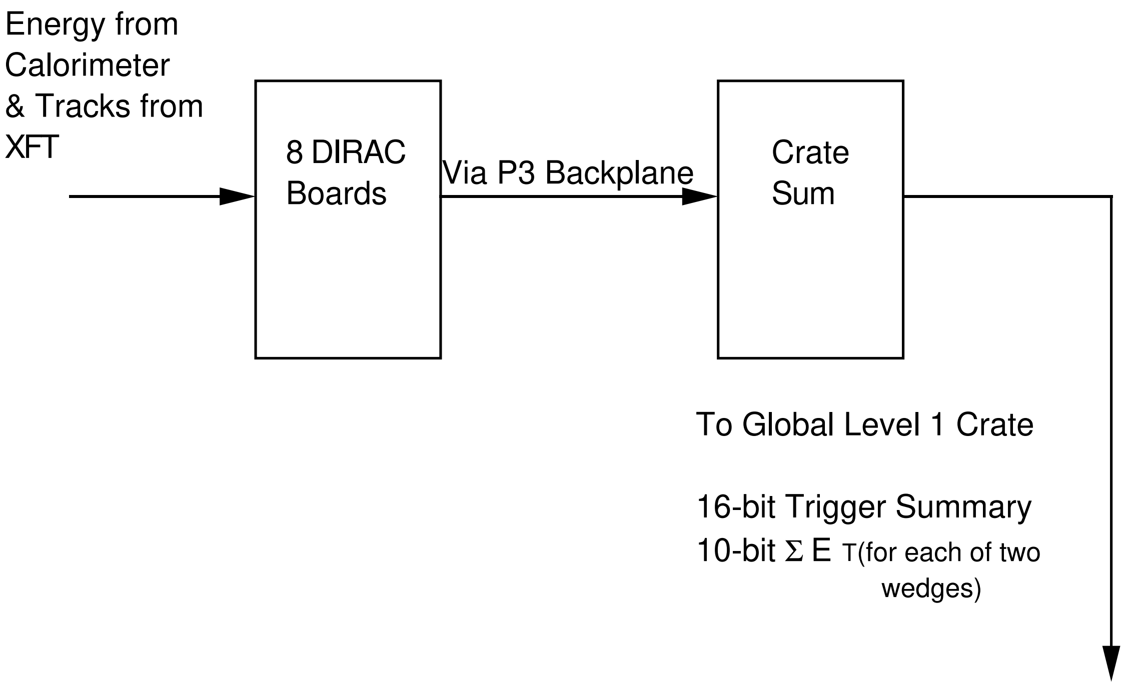

Figure 3: Level 1 Data Flow.

Figure 4: CrateSum Functional Schematic

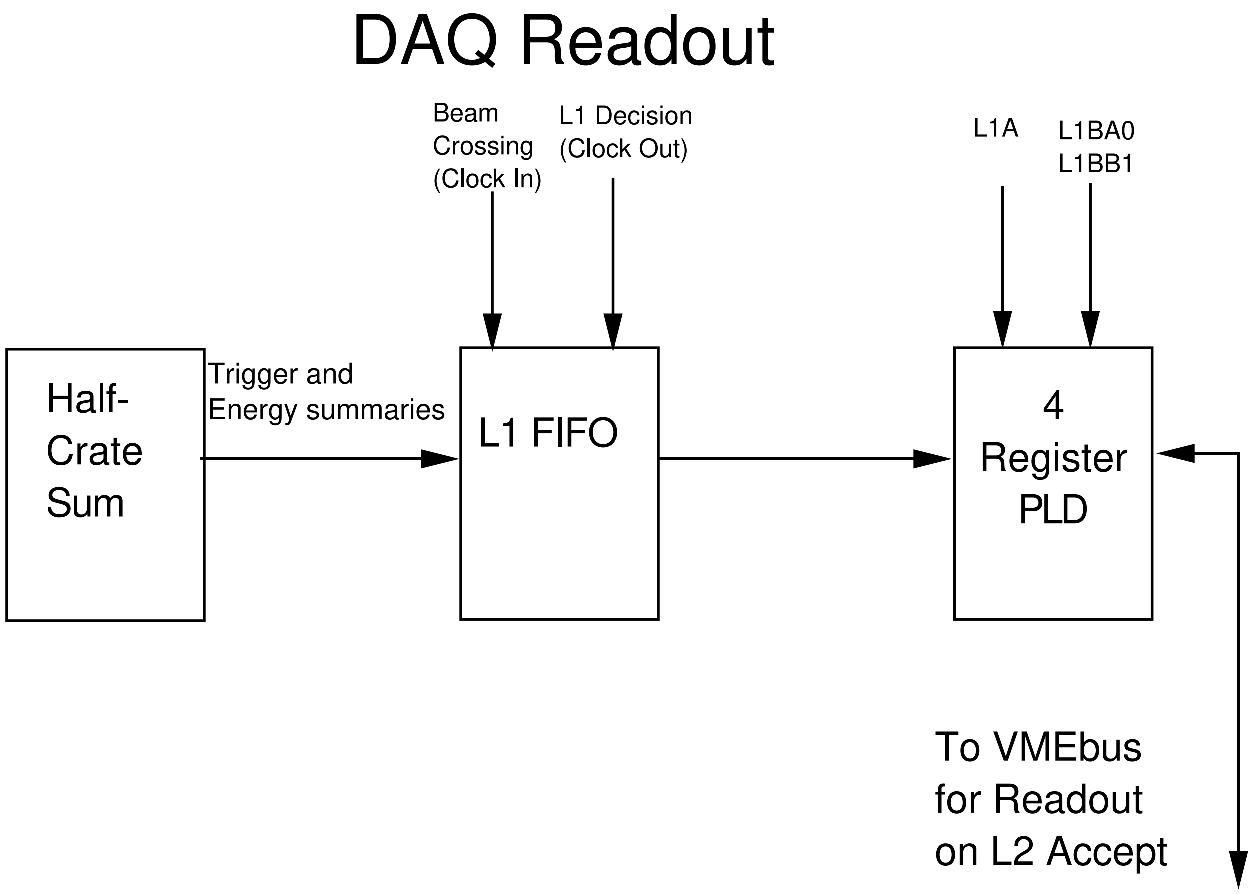

Figure 5: Event Readout Diagram