0.1 The Pace Maker

This describes the current (August 2000) design of the Bunch counter. Some problems have been reported on the operation of this design in the final system. As of this writing, the source of these problems has not yet been identified. Namely wheter they're due to a flaw in this design, or in the CDFCLK and B0 distribution, via the TRACERs, or both.

On schematic sheet 6, right next to the heart is the **Bunch_Counter**, Dirac's pacemaker. Sheet 7 contains the **Bunch_Counter** logic. On the right side of the sheet is the standard **DAQ** L1 FIFO and L2 Buffer for the **BUNCH** data. **BUNCH** counts the number of clocks from an interaction for the event. As data is clocked into the L1 FIFOs around Dirac, the **BUNCH** chip is also clocking data into its L1 FIFO. In this way, if there is a clock distribution problem anywhere in the system, we can quickly diagnose and solve the problem. In TRIGMON, the online trigger monitoring software, the data from all trigger boards will be checked to insure that they all have the same bunch number. Pretty simple!

The schematic for the **BUNCH** chip is called BUNCH.GDF (see BC.ps for a PS version). This design is a fix for the previous version. The problem was in the initial synch of the counter with the B0 marker. The simplest solution is the one addopted here: Have a counter that is always counting CDFCLK and B0, even before h-r-r. Note that one is limited by the existing connections between the chips, and the number of available pins on the BC counter (In this chip, there are still several available)

The CDFCLK input coming *directly* from U104 is negated and used to increment an 8-bit counter. The **_B0** marker comes from the the Shift Register U179, goes to the Heart Chip, where is simply rerouted to here, the Bunch Counter. It resets the 8-bit counter. The D-register 74715 and 8fadd adder are used to set the initial bunch counter offset, within 8 clocks. The values 0-7 are selected via the WO register 700020, see table 13, pg. 30 of [1]. The output of the 74518 comparator is then used to reset the "real" 8-bit counter on the far right, with a phase delay set by the previous mechanism. The bit of logic between the 74518 and the "real" 8-bit counter, ensures that on its output, all the counting numbers stay there for 132 ns. To understand it, take it out, and you'll find that on the COUNT0-7 output, the "0" and the "1" will stay there, for slightly different times, a few ns.

As commented in the design itself, there is a potential problem with this design. The COUNT0-7 output changes every CDFCLK. But refering back to schematics page 7, this output goes to a FIFO that is read by CONTROL67, a delayed CDFCLK by 0, 25, 50 or 75 ns, selectable by the 2 bits TRACKTAP, see see table 17, pg. 35 of [1]. So there is the danger, that the when the FIFO is read, the data is changing. Indeed, probing with the scope, there is some danger for the 75 ns tap, as the data is changing just a few ns before the CONTROL67 read clock.

As per CDF specification, the first word of DAQ readout contains the bunch counter number, board ID and serial numbers.[12] In the lower middle of schematic sheet 6 are a series of jumpers that set the board ID [1] (S2) and serial numbers (S1). These are placed on the board during stuffing of the components. The actual selection of these bits during DAQ readout is part of the memory map. A reported [1] feature of the switches S1 is apparent on the schematics: the switch counting goes as 1 2 3 4 5 6 9 7 8 10, instead of 1 2 3 4 5 6 7 8 9 10. Therefore: to set bit 6 (staring counting at 0) must set switch number 9 (starting counting at 1). To set bit 7, must set switch number 7; to set bit 8, switch number 8.

[1] Dirac board ID is 005 (decimal)

References

[1] Wahl, John E. and Amaral, Pedro *Dirac — The FINAL Specificaton.* CDF/DOC/TRIGGER/CDFR/4225.

[2] Shaw, Teresa M. *Specification for ADC/Memory Module.* Particle Physics Division. CDF Upgrade Project. 6/11/97.

[3] Freeman, Jim, et al. *The Run II eXtrememly Fast Tracker (XFT)* http://cdfsga.fnal.gov/upgrades/daq_trig/xft/xft_home.html.

[4] Toback, Dave. *Crate Sum - Upgrade for Run II.* CDF Trigger Note 91.

[5] The P3 Auxilliary(AUX) card was designed and built by Peter Wilson.

[6] Sarah Truitt is designing the Digital Compare and Sum (DCAS) boards for the Level 2 trigger.

[7] CDF Group, Yale University. *Trigger Supervisor Protocols for Run II* August 18, 1996, Version 1.2.

[8] CDF DAQ Group. *The CDF DAQ Manager's Handbook.* August 18, 1996, Draft #3.

[9] Wahl, John and Wilson, Peter J. *Digital Receive And Compare (DIRAC) Board Startup Timing Diagram.* June 11, 1995, CDF Trigger Note 95.

[10] Peterson, Wade D. *The VMEbus Handbook.* Third Edition. VITA. Scottsdale, AZ, 1993.

[11] VIPA *VME-P Document.* NIM/VME-P 9612.

[12] Ohl, K, Wahl, J, and Wilson, P. *Specification of DAQ/Trigger Synchronization Checking Protocol and VME board Header word.* Version 2.0. CDF/DOC/TRIGGER/CDFR/3145.

[13] Altera Corporation. *Bit Blaster Serial Download Cable Data Sheet.* Altera Corporation Product Data Sheet.