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Interface Specifications for the Level 1 DIRAC Board

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Revisions for 2.0: add delayed B0 and ground pins to XTRP to DIRAC cables, rearrange DIRAC to DCAS connector and switch to 25mil cable for DIRAC to DCAS.

1 Introduction

This note describes the interfaces between the Level 1 DIRAC Boards (and their Auxiliary boards) and the outside world. Section 1 describes the signal specifications for the inputs to the auxiliary card from the frontend cards (ADMEM). Section 2 describes the inputs to DIRAC from the Extrapolation unit (XTRP). Section 3 describes the outputs from DIRAC to the Level 2 cluster finder boards (DCAS). For more details on the DIRAC board see ref [1]. For more information on the Auxiliary card see ref [2].

2 ADMEM to Auxiliary Interface

The input to the Auxiliary card from the frontend ADMEM card has the following specifications:

- 10 differential bits in parallel conforming to LVDS standard (DS90C31 driver/ DS90C32 receiver).
- 20 pin SCSI II connector with metal shell connected to ground on front end card
- Cable Ground connected to connector shell at driver end only
- Signal timing: all signals for all trigger towers to be latched onto the cable simultaneously within a 10 nsec window. Signals will change state no more than once per 132nsec clock cycle.
- Connector pinout as described in Table 1

Table 1: Pin assignments for Auxiliary board Input connectors J0-J11

Pin	Signal	Pin	Signal
1	BIT0	2	$\overline{\text{BIT0}}$
3	BIT1	4	$\overline{\text{BIT1}}$
5	BIT2	6	$\overline{\text{BIT2}}$
7	BIT3	8	$\overline{\text{BIT3}}$
9	BIT4	10	$\overline{\text{BIT4}}$
11	BIT5	12	$\overline{\text{BIT5}}$
13	BIT6	14	$\overline{\text{BIT6}}$
15	BIT7	16	$\overline{\text{BIT7}}$
17	BIT8	18	$\overline{\text{BIT8}}$
19	BIT9	20	$\overline{\text{BIT9}}$

3 XTRP to DIRAC Interface

This specification covers the inputs to the central DIRAC boards. The plug DIRAC boards will have identical input connectors which can receive tracking inputs if there is a source for tracks in the future. There are 2 central DIRAC boards for each 15° wedge so each XTRP output is driven on two identical cables. The cables to the DIRAC card from the XTRP will have the following specifications:

- 10 differential bits in parallel conforming to LVDS standard (DS90C031 driver/ DS90C032 receiver).
- 20 pin standard flat cable with 50mil pitch.
- Each pair will be terminated in 100Ω
- Signal timing: all signals to be strobed onto the cable simultaneously within a 10 nsec window using 132nsec CDF_CLK.
- Connector pinout as described in Table 2

Table 2: Pin assignments for Auxiliary board Input connectors J0-J11

Pin	Signal	Pin	Signal
1	THR1	2	$\overline{\text{THR1}}$
3	THR2	4	$\overline{\text{THR2}}$
5	THR3	6	$\overline{\text{THR3}}$
7	THR4	8	$\overline{\text{THR4}}$
9	THR5	10	$\overline{\text{THR5}}$
11	THR6	12	$\overline{\text{THR6}}$
13	THR7	14	$\overline{\text{THR7}}$
15	THR8	16	$\overline{\text{THR8}}$
17	Delayed B0	18	$\overline{\text{DelayedB0}}$
19	GND	20	GND

4 DIRAC to DCAS Interface

This specification covers the outputs of the DIRAC boards. There are 4 DIRAC boards per 15° wedge and 4 wedges per crate. The DCAS cards that will receive the signals are located in a crate directly above the DIRAC crate. Each DCAS crate holds 12 DCAS cards. Each DIRAC board sends out 3 cables and each DCAS card receives 4 cables. The exact cable routing is specified elsewhere.[3] The cables to the DCAS card from the DIRAC will have the following specifications:

- 40 differential bits in parallel conforming to LVDS standard (DS90C31 driver/ DS90C32 receiver).
- 80 pin Honda RPS–80 connector, using two 80 conductor flat cables with 25mil pitch.
- Signal timing: all signals to be strobed onto the cable simultaneously within a 10 nsec window using 132nsec CDF_CLK.
- Connector pinout as described in Table 3. The entries in the table represent the 10 bit energy information. The first number represents the eta value for the trigger tower and the second indicates the bit (0 ≡lsb). Each cable carries 2 trigger tower energies, electromagnetic and hadron energy for each.

Table 3: Pin assignments for DIRAC cables to DCAS

Pin	Signal	Pin	Signal
A1 (aka 1)	EM0/0	B1 (aka 41)	$\overline{\text{EM0/0}}$
A2	EM0/1	B2	$\overline{\text{EM0/1}}$
⋮		⋮	
A10	EM0/9	B10	$\overline{\text{EM0/9}}$
A11	HAD0/0	B11	$\overline{\text{HAD0/0}}$
A12	HAD0/1	B12	$\overline{\text{HAD0/1}}$
⋮		⋮	
A20	HAD0/9	B20	$\overline{\text{HAD0/9}}$
A21	EM1/0	B21	$\overline{\text{EM1/0}}$
A22	EM1/1	B22	$\overline{\text{EM1/1}}$
⋮		⋮	
A30	EM1/9	B30	$\overline{\text{EM1/9}}$
A31	HAD1/0	B31	$\overline{\text{HAD1/0}}$
A32	HAD1/1	B32	$\overline{\text{HAD1/1}}$
⋮		⋮	
A40 (aka 40)	HAD1/9	B40 (aka 80)	$\overline{\text{HAD1/9}}$

References

[1] J. Wahl, *Digital Raw - An Overview*, CDF Trigger note TGN-90, (1993).

[2] P.J. Wilson, , CDF Trigger note TGN-92, (1993).

[3] J. Wahl and P.J. Wilson, , CDF Trigger note TGN-??, (1995).