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# Digital Receive And Compare (DIRAC) Board Startup Timing Diagram

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The intent of this note is to describe the timing sequence involved in synchronizing the L1 calorimeter trigger cards at the beginning of a run or after a hardware error has been received by the Trigger System Interface (TSI)[1]. This synchronization uses the famous "HALT-RECOVER (RESET) - RUN" sequence[2].

Figure 1 shows a simplified timing diagram for the Digital Information Receive And Compare (DIRAC) board[3]. The first two signals are derived from accelerator signals by the Clock. The Clock sends them to a TRACER module[4] in the crate which then transmits them over the P2 backplane to the individual cards[5]. The **CDF_CLK** has a 132ns cycle and runs continuously. All the signals from the clock or the TSI/TRACER other than the **CDF_CLK** are used as gates on the clock: the timing is set by the leading edge of **CDF_CLK**. The **B0** signal comes once every cycle around the ring or once every 159 **CDF_CLK**s. In the figure the numbers in the **CDF_CLK** indicate how many cycles have occurred since the *first* **B0** after the HALT-RECOVER-RUN sequence.

The sequence starts when the **HALT** signal is sent. When the **HALT** is received all clocking of data on the DIRAC board stops: FIFOs are halted, trigger processing stops etc. Data may still flow up from the calorimeter frontend board (ADMEM) but it is not latched into the DIRAC card and is ignored. In the **HALT** state, registers and FIFOs on DIRAC can be readout over VME for diagnostic purposes. At some later time the **RECOVER** signal (formerly RESET) signal is sent. On receipt of this signal all FIFOs on the board and the B0 counter are reset. The length of this reset cycle is set by a timer in the TSI and is expected to be about 10ms. At the end of the reset cycle the TSI sends a **RUN** signal which is interpreted by the TRACER which then drops the **HALT** line. This is interpreted by the DIRAC board as an arming signal to prepare to start. The board starts clocking when it receives the first **B0** signal after **HALT** ends. To allow the boards to get ready, the TSI guarantees that the **RUN** signal will come at least 35 clock cycles before the next **B0** signal.

After the **HALT-RECOVER-RUN** sequence has been executed all the systems start collecting data. However the event associated with the **B0** will not reach the DIRAC card until about 12 clock cycles later. During this time the DIRAC board does not clock any data in. It starts to clock the Input Latch when it expects the first valid data and continues every 132ns until the next **HALT** (end of run, error recovery...) signal. Once the first data has been processed it is stored in the L1 readout FIFO using **L1_FIFO_IN**. This data will be clocked out the FIFO when the first L1 decision is received from the TSI. The **L1_FIFO_OUT** signal is the logical "OR" of **L1A** and **L1R**.

Since the decision on a given event is received 42 clocks after the crossing occurred in the detector this is when the data is clocked out of the FIFO. To avoid prematurely clocking the data out of the L1 FIFO *no L1 accepts (***L1A***) or L1 rejects (***L1R***)* are sent by the TSI from the beginning of the Halt until 42 cycles after the **B0** associated with the **RUN** signal. From that point until the next **HALT** signal, the TSI sends either a **L1A** or a **L1R**. In 396ns operation, the system runs with a 132ns clock cycle but the clock cyles which have no associated beam crossings get automatic rejects associated with them.

# References


[1] CDF Group/Yale University, *Conceptual Design of the Trigger System Interface for the Run II Upgrade*, Yale Trigger NOte #1, 1995.

[2] CDF Group/Yale University, *Trigger Supervisor Protocols for RUN II*,1996.

[3] J. Wahl and Y. Fridman, *Digital RAW - An Overview*, TGN-90, 1994.

[4] T. Shaw, *Specifications for the TRigger And Clock + Event Readout Module (TRACER)*, 1993-95.

[5] T. Shaw and G.Sullivan, *A CDF standard VME readout crate for the Upgrade*, CDF/DOC/TRIGGER/CDFR/2388, 1993.

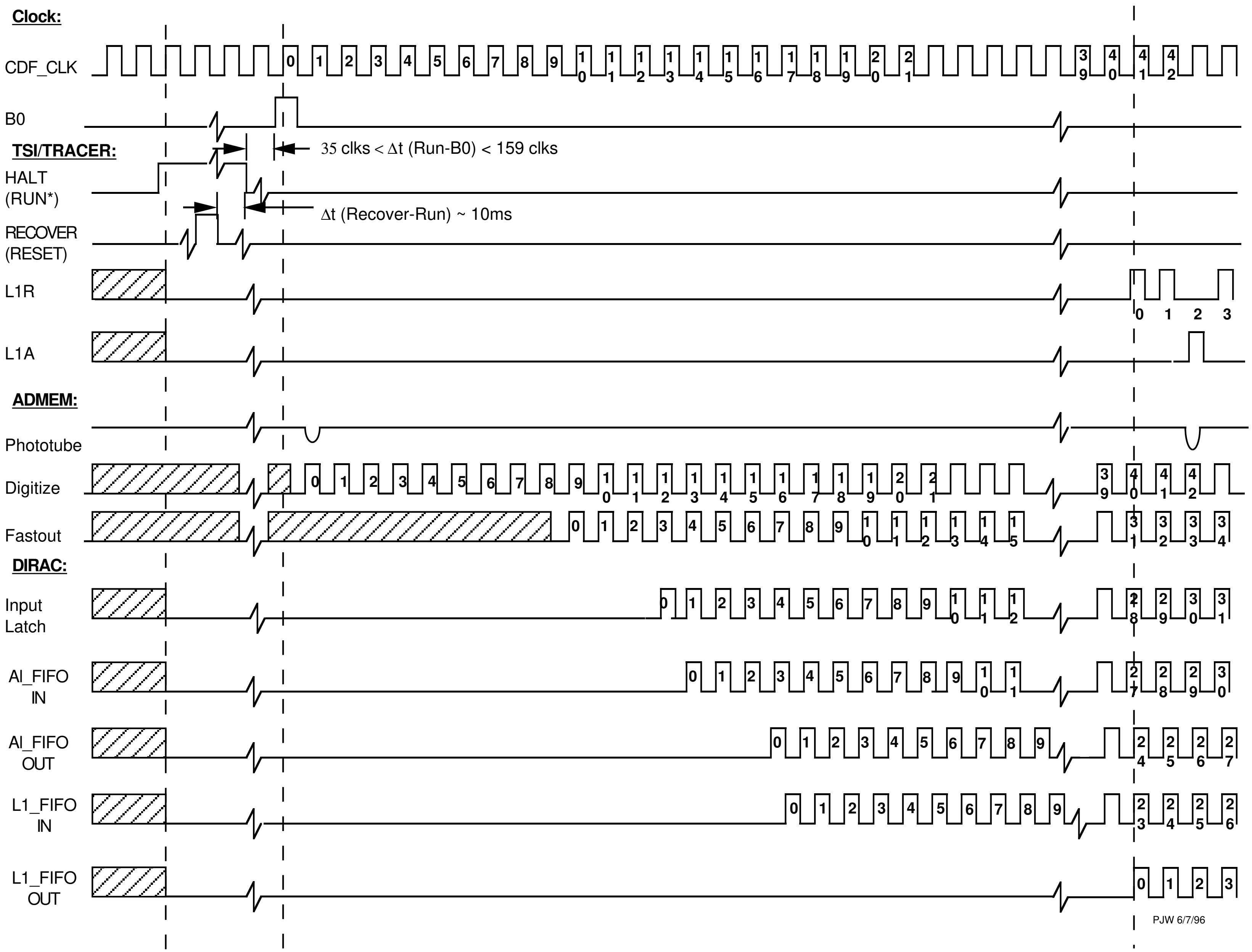


Figure 1: Startup timing diagram for the DIRAC board.